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A 1-to-4 SiGe BiCMOS Analog Demultiplexer Sampling Front-End for a 116 GBaud-Receiver

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***Abstract* — This paper presents a 116 GS/s analog demultiplexer front-end, sampling one differential input channel and routing it cyclically to 4 differential outputs at 29 GS/s each. With this topology, analog-to-digital converters can be time-interleaved to build a digitizing system with more than 100 GBaud, while keeping the necessary bandwidth under 15 GHz. Especially CMOS analog-to-digital converters benefit from this relaxed bandwidth requirement, which enables cost-efficient 116 GBaud silicon receivers for optical communications and instrumentation.**

***Keywords* — analog-digital conversion, analog integrated circuits, bicmos integrated circuits, demultiplexing, sampled data circuits, silicon germanium.**

I. Introduction

Massive digitization efforts push data networks to their limits. While optical fibers still have significant amount of unused bandwidth, it is the electronic receiver that limits maximum data rates per wavelength. Utilizing considerable amounts of wavelengths simultaneously can avoid the data traffic congestion, but is costly. For the rollout of 5th- and the development of 6th-generation mobile communication infrastructure, backhauling networks as well as real-time instruments for characterization need higher available bandwidths in the electronic receivers. Since analog bandwidths in single-core analog-to-digital converters (ADC) remain below 40 GHz, time-interleaving is the only viable option to achieve more than 80 GBaud. Another benefit of lower data rate ADCs is the potentially higher accuracy. Commonly used modulation schemes in coherent optical networks are 16-QAM or 64-QAM, with 4–6 bits used per ADC, including room for equalization. Spectral efficiency could improve greatly with higher resolution of the time-interleaved receivers. The presented circuit aims at aiding in the realization of such systems. Chapter 2 briefly describes the circuit architecture; experimental results are presented in chapter 3 and compared to state-of the-art SiGe sampling circuits in chapter 4. The paper is concluded in chapter 5.

II. Circuit Architecture

A. Charge-Sampling Integrator Core

The principle architecture follows the charge-sampling approach as employed by other high-bandwidth sampling circuits [1], [2]. A transconductance amplifier converts the input voltage into an equivalent input current. This current is then steered into the active branch, where the clock signal clk is on high level while the active branch tracks the input signal. Above the switching layer, the signal current is charging a hold capacitance C_H of 60 fF, introducing a voltage difference on the two terminals of C_H in the integration phase (I). This capacitance then holds the output voltage constant during hold phase (H), until the differential reset signal res is set to a high level. A switched emitter follower then sets the voltage on C_H back to a defined level and thereby removes the signal-induced charge to avoid inter-symbol interference. After this reset phase (R), a new sampling cycle begins.

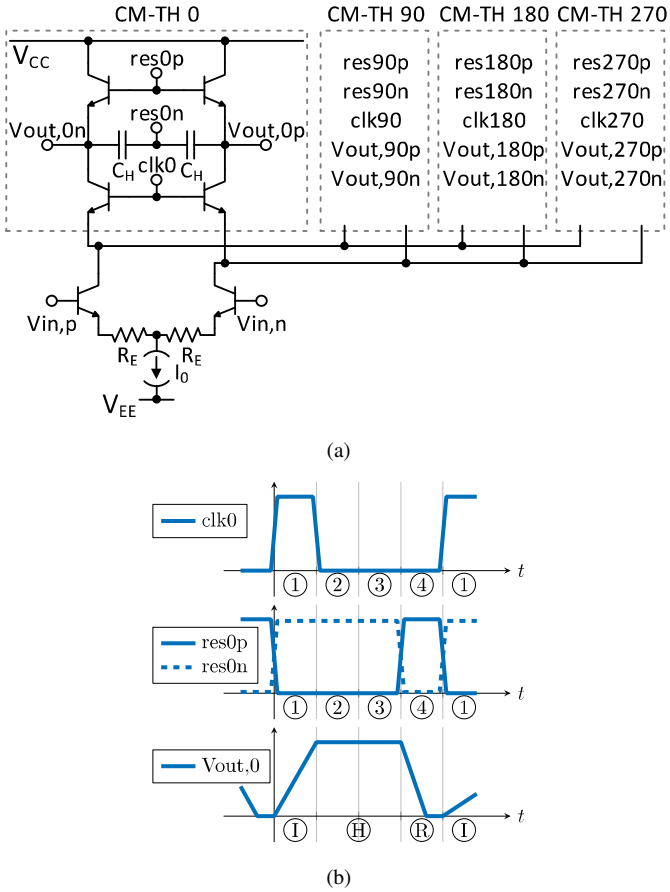

Fig. 1. Integrator core schematic with input transconductance amplifier and 4 current-mode track-and-hold (CM-TH) circuits (a) and principle switching signals for clock, reset and output of channel 0° (b).

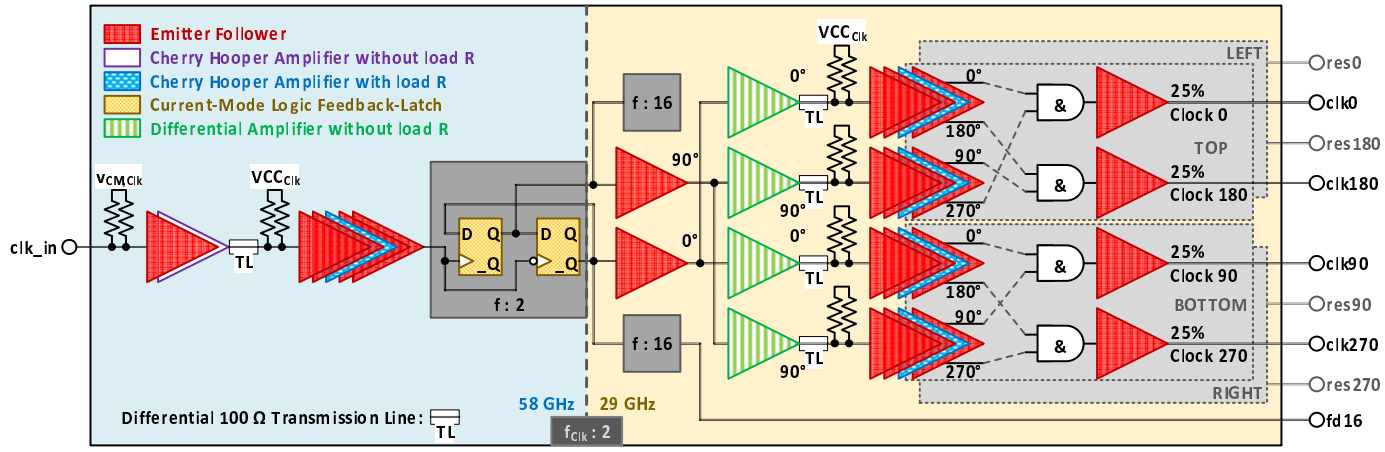

Fig. 2. Block diagram of the fully differential circuit block, conditioning the quadrature 29 GHz clock- and reset signals with 25% duty-cycle from a differential 58 GHz sine-wave input. The frequency divider consists of more pairs of CML feedback-latches and provides the 1.8125 GHz trigger signal (*fd16*, bottom) and layout symmetry (dummy at the top).

The timing of the 3 sampling phases is set to 25% for I and R and to 50% for H, referring to the single-channel sampling rate of 29 GS/s. Consequently, when all 4 output channels are combined, the charge-sampling analog demultiplexer has the output signal of a single-core 116 GS/s sample-and-hold. A schematic of the circuit and the described switching signals is shown in Fig. 1. The subsequent output buffers are not shown and consist of a 3.6 mA emitter follower, to draw as little current as possible from C_H, and a 12 mA differential amplifier for common-mode rejection. The tail current of each channel's output buffer can be tuned individually to account for gain mismatch. The input buffer is another 4 mA emitter follower, inputs and outputs are terminated with 50 Ω resistors and differential 100 Ω transmission lines lead to the I/O pads.

An advantage of the current-mode sampling is not only the high bandwidth and signal quality for high frequencies, but also the possibility to easily modify the input stage for direct connection to the current outputs of a differential photodiode. The signal current would then be connected in parallel to the tail current source. By omitting the transimpedance amplifier in between, a larger degree of integration could be reached and eventually, the whole optoelectronic receiver front-end might be integrated on a single chip.

B. Clock and Reset Signal-Conditioning

A block diagram of the clock and reset signal-conditioning circuit is pictured in Fig. 2. Other than in [2], we employ a single-stage clock switch instead of a dual-stage switching layer. While the latter has one switching stage with low frequency corresponding to the single-channel sampling rate $f_S/4$ and one with high frequency at $f_S/2$, the clock signal generation is relaxed due to the 50% duty-cycle. However, two stacked transistor layers are necessary to implement this topology, the switching instants must carefully be adjusted and the longer current path suffers from additional attenuation and hence, lower bandwidth.

The single-stage switching layer with 25% duty-cycle at the single-channel sampling rate of $f_S/4$ can be implemented with just one transistor switch, which lowers the required supply voltage at least by the base-emitter voltage v_{BE} and the clock signal amplitude $\hat{v}_{clk}$. The next channel takes over the signal current when its clock signal rises above the clock level of the previous channel like in a differential amplifier, only with 4 input transistors. No special timing is required, since gain mismatches can still be adjusted at the output buffers of each channel. The short delay time and high input bandwidth are essential for implementing a receiver system with ultra-high data rates above 100 GS/s. The single-core current-mode track-and-hold amplifier in [1] already demonstrated promising results with a normalized attenuation of only -1.1 dB at 40 GHz. The necessary circuitry for 25% duty-cycle clock-signal shaping consumes additional DC power, which has to be considered as a disadvantage, although it is compensated by increased performance.

Due to the large number of amplifying circuits in the clock path, the clock- and reset-driver is very sensitive, yet robust. This can be confirmed in measurements, where it operates on the signal generator's largest as well as the lowest amplitude setting of +9 dBm and -20 dBm, respectively, without need for deembedding additional losses in the measurement equipment. A chip photograph can be found in Fig. 3. We used Infineon Technologies' 130 nm BiCMOS technology B11HFC with f_T and f_{max} of 250 GHz and 400 GHz, respectively.

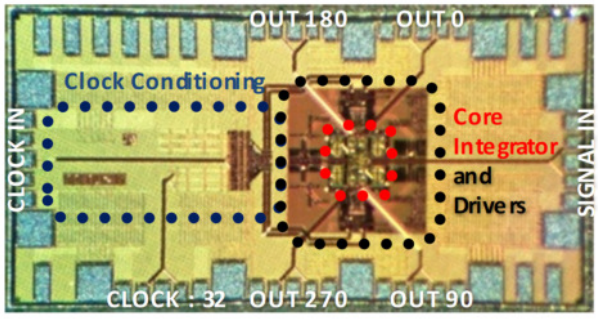

Fig. 3. Chip photograph of the charge-sampling analog demultiplexer. Dimensions are 3.10 mm x 1.55 mm and limited by pad layout for wafer-prober measurements.

III. Measurement Setup and Experimental Results

The chip is measured with a wafer-prober and a GSGSG-probe configuration. An Anritsu 69397B delivers the 58 GHz clock signal, whereas a Rohde&Schwarz SMF100A provides the input signal up to 43.5 GHz. A Marki Microwave BAL-0067 balun transforms the single-ended generator output into a differential signal, the positive clock input is excited single-ended with a 50 Ω termination on the negative clock input. A Tektronix DSA8300 captures the output signal with an 80E11 differential sampling module set to 70 GHz bandwidth. The trigger signal is provided by the chip's frequency divider output. Therefore, only outputs 0° and 180° can be measured, as can be seen from Fig. 3. All instruments are coupled by the 10 MHz reference of the clock signal generator and protected from the chip's operating point by DC blocks.

Experimental results are shown for output channel 0° with a single-channel sampling rate of 29 GS/s, corresponding to an overall system sampling rate of 116 GS/s. Fig. 4 shows the transfer characteristic at the trigger frequency of 1.8125 GHz with a 1 dB-compression point of 9 dBm. The distortion up to the 5th harmonic is presented in Fig. 5 with a maximum SFDR of 44 dBc and a minimum THD of -41 dB. Fig. 6 gives the accuracy calculated from THD and from the distortion of all frequency components. Since we used 64 x averaging, the latter cannot truly be referred to as SNDR, since it suppresses both oscilloscope and chip noise. A maximum of 6.6 ENOB can be observed at low input swings, whereas Fig. 7 shows max. 4.4 ENOB at a higher signal frequency of 27.1875 GHz, $^{15}/_{16}$ of the single-channel sampling rate. At 1.0 V_{pp}, both input frequencies allow an accuracy of more than 4 ENOB. Fig. 8 and Fig. 9 present the captured transient signal and the corresponding frequency spectrum at the lower frequency, respectively. Eventually, the results are summarized in Table 1.

Table 1. Performance summary of the charge-sampling analog demultiplexer.

Max. Sampling Rate	4 x 29 GS/s = 116 GS/s
Max. SFDR	44 dBc @ 1.8125 GHz 29 dBc @ 27.1875 GHz
Min. HD3	-44 dBc @ 1.8125 GHz -45 dBc @ 27.1875 GHz
Min. THD	-41 dB @ 1.8125 GHz -28 dB @ 27.1875 GHz
Max. ENOB from THD	6.6 @ 1.8125 GHz 4.4 @ 27.1875 GHz
Input Voltage Range	1.0 $V_{pp,diff}$ for > 4 $ENOB_{THD}$
P1dB / IIP3 @ 1.8125 GHz	9 dBm / 5 dBm
Supply Voltage	4.7 V / 4.6 V
Total Chip / Core Power	5.5 W / 1.8 W
Total Chip / Core Area	4.8 mm² / 0.12 mm²
Technology f_T / f_{max}	130 nm SiGe BiCMOS 250 GHz / 400 GHz

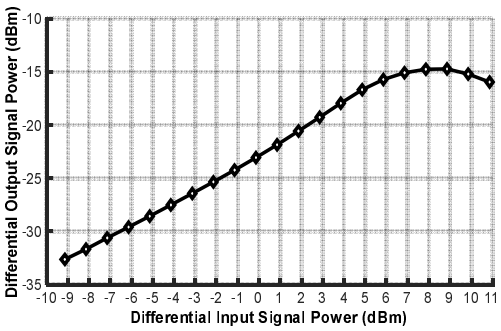

Fig. 4. Measured differential output vs. input signal power of channel 0° at 1.8125 GHz and 29 GS/s (116 GS/s overall). RF probes are not de-embedded.

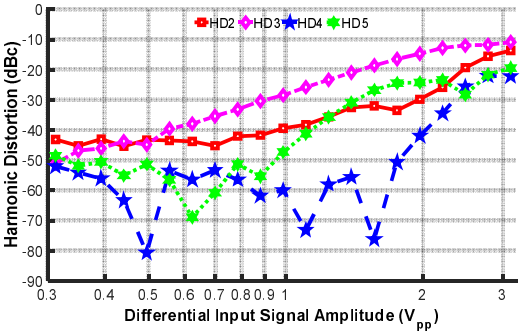

Fig. 5. Measured harmonic distortion of the first five harmonics of channel 0° at 1.8125 GHz and 29 GS/s (116 GS/s overall).

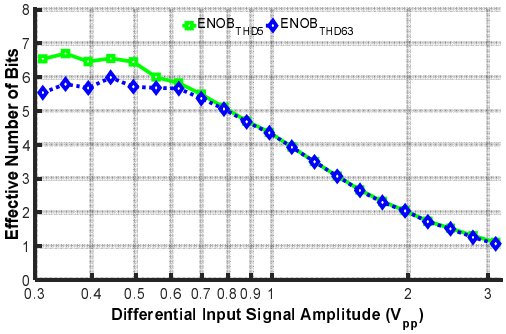

Fig. 6. Measured effective number of bits (ENOB) of channel 0° at 1.8125 GHz and 29 GS/s (116 GS/s overall), calculated from measured THD of the first five harmonics (THD_5) and all 63 frequency components (THD_{63}).

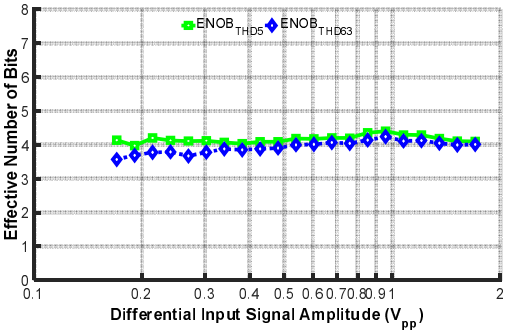

Fig. 7. Measured effective number of bits (ENOB) of channel 0° at 27.1875 GHz and 29 GS/s (116 GS/s overall), calculated from measured THD of the first five harmonics (THD_5) and all 63 frequency components (THD_{63}).

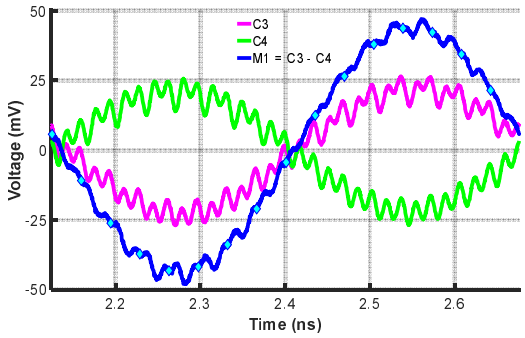

Fig. 8. Captured time-domain plot of the single-ended and differential output signal of channel 0° at 1.8125 GHz and 29 GS/s (116 GS/s overall) with highlighted sampling instants for 0.44 V_{pp} differential input swing.

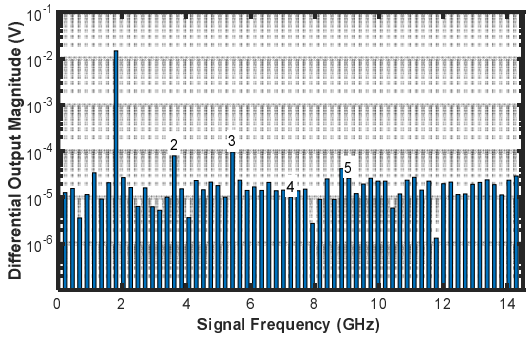

Fig. 9. Calculated frequency-domain plot of a 128-point DFT of the sampled differential output signal of channel 0° at 1.8125 GHz and 29 GS/s (116 GS/s overall) with highlighted harmonics for 0.44 V_{pp} differential input swing.

IV. Comparison to State-of-the-Art

Table 2 gives an overview of related state-of-the-art analog sampling front-ends in high-performing SiGe BiCMOS technologies. The track-and-hold amplifier in [1] uses the same core integrator topology and demonstrates the single-core performance at 25.6 GS/s. Another charge-sampling analog demultiplexer was published in [2] with a dual-switching layer. It shows excellent performance at almost the same sampling rate with a more advanced SiGe BiCMOS technology. The same holds for the single-core track-and-hold amplifier in [3]. Although the latter consumes much less power, the charge-sampling analog demultiplexer presented in this work can provide higher overall sampling rate alongside an accuracy of 4 bits at almost twice the max. measured signal frequency. In addition, it can utilize 29 GS/s analog-to-digital converters with a relaxed bandwidth requirement of only 14.5 GHz, which makes it well-suited for commercially available CMOS converters and FPGA interconnects, which would make it a cost-efficient silicon receiver system.

V. Conclusion

We demonstrate a charge-sampling analog demultiplexer front-end for 116 GBaud applications with 4 bits of accuracy. It shows not only the highest sampling rate in SiGe BiCMOS technology, but is also the first sampling system to achieve more than 100 GS/s with less than 300 GHz of f_T. We are confident to achieve similar or better results at reduced power consumption in the future, with the next generation of this high-performing technology. With relaxed bandwidth requirements, a powerful receiver system for optical communications or instrumentation with more than 100 GBaud and up to 400 Gbit/s can be implemented economically with commercially available CMOS ICs and FPGA-components.

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Table 2. Comparison to related state-of-the-art SiGe BiCMOS sampling front-ends.

Reference	**[1]**	**[2]**	**[3]**	**This Work**
Sampling Rate	25.6 GS/s	4 x 28 = 112 GS/s	90 GS/s*)	**4 x 29 = 116 GS/s**
Input Voltage Swing	0.5 V_{pp}	0.5 V_{pp}	0.8 V_{pp}	**0.5 V_{pp}**
Max. SFDR	48 dBc @ 1 GHz 33 dBc @ 40 GHz	44 dBc @ 1 GHz 35 dBc @ 38 GHz	55 dBc @ 1 GHz 43 dBc @ 15 GHz	**44 dBc @ 1.8 GHz** **29 dBc @ 27.2 GHz**
Min. THD	-44 dB @ 1 GHz -32 dB @ 40 GHz	-36 dB @ 1 GHz**) -28 dB @ 43 GHz**)	-49 dB @ 1 GHz -38 dB @ 15 GHz	**-41 dB @ 1.8 GHz** **-28 dB @ 27.2 GHz**
Supply Voltage	3.5 V / 5.5 V	3.5 V / 6.5 V	2.5 V / 1.8 V	**4.7 V / 4.6 V**
Total / Core Power Consumption	0.913 W / 0.123 W	3.3 W / 2.3 W	0.087 W / 0.020 W	**5.5 W / 1.8 W**
Technology **f_T / f_{max}**	130 nm SiGe BiCMOS 250 GHz / 400 GHz	130 nm SiGe BiCMOS 300 GHz / 450 GHz	55 nm SiGe BiCMOS 330 GHz / 350 GHz	**130 nm SiGe BiCMOS** **250 GHz / 400 GHz**

*) Sampling functional up to 108 GS/s, SFDR and THD given for up to 90 GS/s; **) Including noise, assuming THD = -SNDR