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A SiGe-HBT 2:1 Analog Multiplexer with more than 67 GHz Bandwidth

Tobias Tannert, Xuan-Quang Du, Daniel Widmann, Markus Grözing, Manfred Berroth
Institute of Electrical and Optical Communications Engineering
University of Stuttgart, Germany
tobias.tannert@int.uni-stuttgart.de

Christian Schmidt, Christoph Caspar, Jung Han Choi, Volker Jungnickel, Ronald Freund
Fraunhofer Heinrich Hertz Institute
Berlin, Germany

***Abstract*—This paper presents a 2:1 Analog Multiplexer (AMUX) in a SiGe-HBT technology. The AMUX is used for time interleaving operation of two digital-to-analog converters (DACs) and therefore extends both the sampling rate and the bandwidth compared to a single DAC. The linear AMUX signal path allows for generation of broadband signals with higher order modulation schemes which is essential for raising data rates in optical communication networks. The AMUX provides a differential peak-to-peak output voltage of up to 1 V with linear gain. A signal path 3-dB bandwidth exceeding 67 GHz has been measured. The clock path exhibits a 3-dB bandwidth of 60 GHz. S-parameter measurements are presented. Measured PAM4 eye diagrams at 56 GS/s from the time interleaving operation of two DACs are reported.**

***Index Terms*—Analog multiplexer (AMUX), Silicon-germanium (SiGe), Heterojunction bipolar transistor (HBT), Time interleaving**

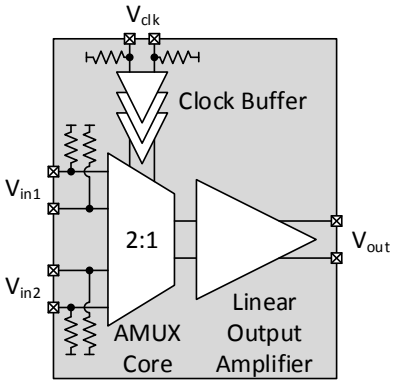

Fig. 1. Block diagram of the 2:1 AMUX.

I. Introduction

To fulfill the ever growing demand for higher data rates in optical communication networks both higher symbol rates and higher modulation schemes have to be applied. This demands for digital-to-analog converters (DACs) showing high sampling rates, high output bandwidth and high vertical resolution.

To realize high sampling rate PAM signals different time interleaving concepts are used. If only PAM2 modulation is desired the circuit can be implemented in the digital domain and high sampling rates are achieved by very fast digital multiplexers [1]. For higher order modulation schemes a combination of digital multiplexing followed by a single D/A output network is often used resulting in sampling rates up to $100\,\mathrm{GS/s}$ and bandwidths of more than $40\,\mathrm{GHz}$ [2]–[4]. Time interleaving of multiple sub-DACs can also be done in the analog domain. One example of two time interleaved sub-DACs with directly combined output signals in a single integrated circuit (IC) is shown in [5], yielding a $100\,\mathrm{GS/s}$ sampling rate.

Another promising approach pursued in this work is time interleaving of sub-DACs by means of an Analog Multiplexer (AMUX). A major benefit of this approach is that the bandwidths of the sub-DACs can be aggregated, presuming the bandwidth of the AMUX itself is high enough. For example the benefits of CMOS and bipolar semiconductor technologies can be combined by time interleaving of CMOS DACs with an AMUX using bipolar transistors. CMOS DACs are well suited for integration of digital signal pre-processing but show a limited bandwidth. This drawback can be overcome by the use of an AMUX in a bipolar technology that is beneficial for high bandwidth analog front end circuits. AMUX ICs in InP technologies have been presented in [6] and [7], the latter offering a signal path transmission bandwidth beyond $50\,\mathrm{GHz}$.

The circuit presented in this paper is a 2:1 AMUX in a SiGe-HBT technology that selects one of two analog input signals with a sampling clock. The selected input signal appears at the output of the linear signal transmission path. This allows for time interleaving and bandwidth aggregation of two input devices at very high sampling speed.

In section II the AMUX circuit is presented. Section III shows the frequency domain S-parameters as well as time domain simulation and measurement results. The paper is concluded in section IV.

II. Circuit Design

The AMUX circuit is implemented in the SiGe-HBT BiCMOS technology SG13G2 from IHP which features high speed bipolar transistors with a maximum transit frequency of $f_\mathrm{T} = 300\,\mathrm{GHz}$ and a maximum oscillation frequency of $f_\mathrm{max} = 500\,\mathrm{GHz}$ [8].

Fig. 1 shows a block diagram of the IC. The circuit design is fully differential with an input and output port differential impedance of $100\,\Omega$. A voltage gain of $A_\mathrm{V} = 1$ and linear

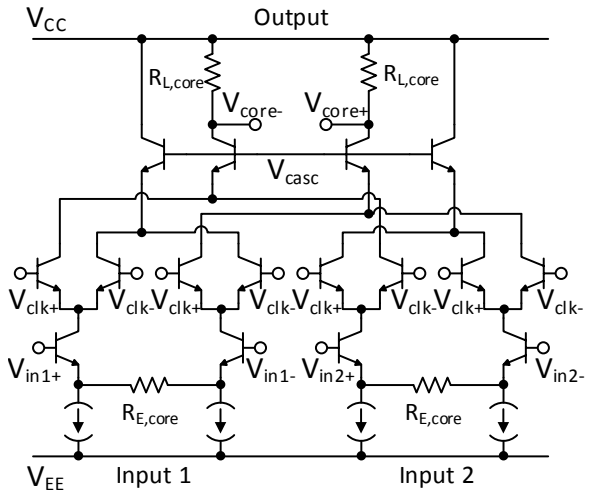

Fig. 2. Schematic of the 2:1 AMUX core.

gain is obtained for input signals with a maximum differential peak-to-peak voltage of 1 V. The AMUX core that combines the input signals is driven by a multi stage clock buffer and followed by a linear output amplifier. The additional output amplifier driving the 100 Ω output allows for the use of smaller transistors and resistors in the AMUX core resulting in a more compact design with less parasitics in this critical part. This enables a high bandwidth. The impedance controlled coplanar microstrip lines at the inputs and output and between the distributed clock buffer stages have been designed with the help of electromagnetic (EM) field simulations. The individual functional blocks of the AMUX are described below.

A. Clock Buffer

The clock buffer consists of multiple high-gain Cherry-Hooper amplifiers with emitter followers between each stage. A simulated small signal voltage gain of 41.6 dB is reached for low frequencies. The last stage of the clock buffer is inductively peaked to provide for large swing and steep slopes at the AMUX current switches. The simulated limited and settled peak-to-peak differential output voltage swing of the clock buffer is 520 mV.

B. MUX Core

The schematic of the AMUX core is shown in Fig. 2. Differential transconductance amplifiers which are linearized with emitter degeneration resistors $R_{\mathrm{E,core}}$ are placed at the signal inputs (V_{in1}, V_{in2}). The input termination and additional emitter followers at the signal inputs before the transconductance amplifiers are not shown in the schematic. The signal currents pass through clocked current switch pairs that perform the selector operation. In the state $V_{\mathrm{clk+}} = \mathrm{H}$, $V_{\mathrm{clk-}} = \mathrm{L}$, the signal currents of input 1 are switched to the output, whereas the signal currents of input 2 are switched to a dummy load. The state $V_{\mathrm{clk+}} = \mathrm{L}$, $V_{\mathrm{clk-}} = \mathrm{H}$ is vice versa. The output comprises cascode transistors and load resistors $R_{\mathrm{L,core}}$ generating the core output voltages $V_{\mathrm{core+}}$ and $V_{\mathrm{core-}}$.

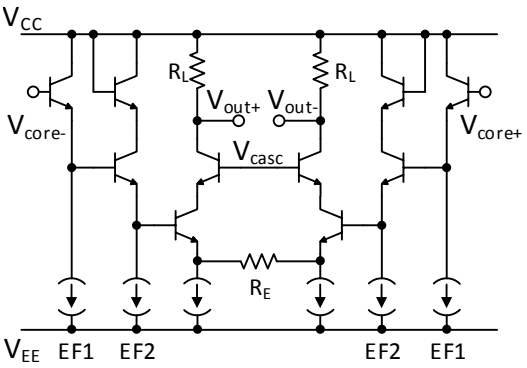

Fig. 3. Schematic of the output amplifier.

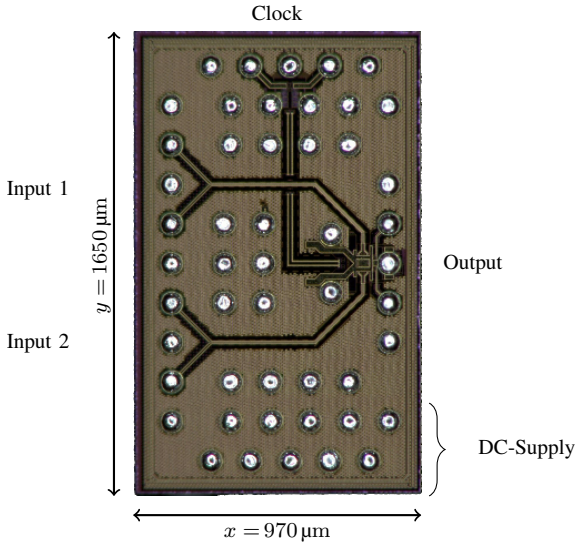

Fig. 4. Chip photograph of the 2:1 AMUX.

C. Output Amplifier

Fig. 3 shows the schematic of the output amplifier. The amplifier has a linear voltage gain of $A_{\mathrm{V,amp}} = 2$ to compensate for the voltage gain of the AMUX core which is $A_{\mathrm{V,core}} = 0.5$. This results in an overall gain of $A_{\mathrm{V}} = A_{\mathrm{V,core}} \cdot A_{\mathrm{V,amp}} = 1$ for the whole signal path. At the amplifier input two series connected emitter followers (EF1, EF2) are used as buffers, level shifters and for some peaking of the amplifier frequency response. At the output there is a differential transconductance cascode stage with emitter degeneration linearization by R_{E}. The load resistors R_{L} are 50 Ω for output matching to the differential 100 Ω system. The constant part of the output stage current is fed through external DC-feeds at the output pins, hence only the alternating current flows through the load resistors. Thus, the load resistors can be designed with a reduced area which reduces the capacitance at the output. Adjusting the single output amplifier stages' bias currents allows for fine tuning of the output frequency response.

III. Simulation and Measurement Results

Fig. 4 shows a photograph of the fabricated chip that is prepared for flip-chip assembly. The chip size is $970\,\mu\text{m} \times 1650\,\mu\text{m}$. Operating voltages are $V_{\text{CC}} = 0\,\text{V}$ and $V_{\text{EE}} = -4.5\,\text{V}$ for the AMUX core as well as the output amplifier and $V_{\text{EE,clk}} = -3.4\,\text{V}$ for the clock buffer respectively. The total power consumption is $1.06\,\text{W}$. All measurements are done directly on-chip (before bumping).

The simulation model of the AMUX consists of RLC extracted netlists of all circuit blocks and EM simulation models for all transmission lines.

A. Frequency Domain

The S-parameter measurements are carried out as 2-port measurements in the differential mode of the network analyzer (NWA). The measurement frequency range is between $689.8\,\text{MHz}$ and $67\,\text{GHz}$. Fig. 5 shows the measurement setup for the signal path through input 1. In this case port 1 of the NWA is connected to the input 1 of the AMUX and port 2 of the NWA is connected to the AMUX output. For the measurements of the signal path through input 2 this input is denoted as port 3. For the measurements of the clock path the clock input is denoted as port 4. During the signal path measurement as shown in Fig. 5 the clock inputs are set to an appropriate DC voltage so that the measured signal path is either transparent or isolating.

The simulated and measured reflection coefficients for the two signal inputs and the output are shown in Fig. 6. All measured reflection coefficients are better than $-10\,\text{dB}$ in the considered frequency range. Fig. 7 shows the transmission coefficients of the transparent signal path for both inputs. The shape of the measurement results matches the small signal simulation very well with a constant offset of $2.75\,\text{dB}$. A reduced bias current in the output amplifier during the measurements is supposed to cause this offset. The attenuation of the transmission parameter increases by $2.2\,\text{dB}$ from low frequencies up to $67\,\text{GHz}$, thus, the signal path 3-dB bandwidth exceeds $67\,\text{GHz}$. Due to the signal path linearity the results are very similar for the measured differential power levels of $+1\,\text{dBm}$ to $-17\,\text{dBm}$ at $100\,\Omega$. The attenuation of the isolated signal paths is better than $-29\,\text{dB}$ in the measured frequency range.

For the measurement of the clock path the signal input 1 is biased at a constant voltage of $V_{\text{in1D}} = +600\,\text{mV}$ and input 2 is biased at $V_{\text{in2D}} = -600\,\text{mV}$. The measured transmission coefficient of the clock path is shown in Fig. 8 for a differential input power of $P_{\text{in}} = 0\,\text{dBm}$ at $100\,\Omega$. The large signal 3-dB bandwidth is approximately $60\,\text{GHz}$.

B. Time Domain

The time domain measurement setup is depicted in Fig. 9. Time interleaving operation of two DACs with the AMUX is evaluated. The SHF 613A DACs [9] feature an analog output bandwidth of $36\,\text{GHz}$. A bit pattern generator (BPG) delivers 2-bit samples for each DAC. The DACs are run with a phase offset of $180°$. To achieve optimal sampling points for the

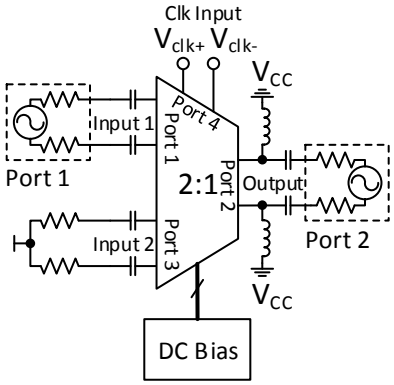

Fig. 5. S-parameter measurement setup for signal path.

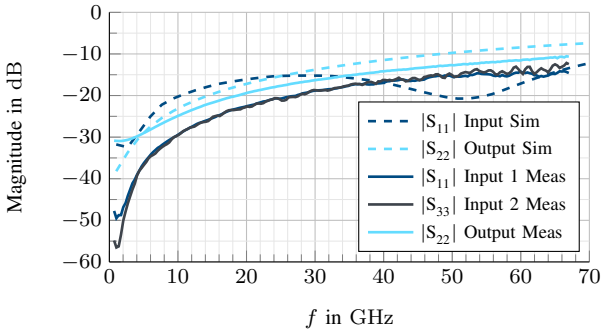

Fig. 6. Simulated and measured input and output reflection coefficients.

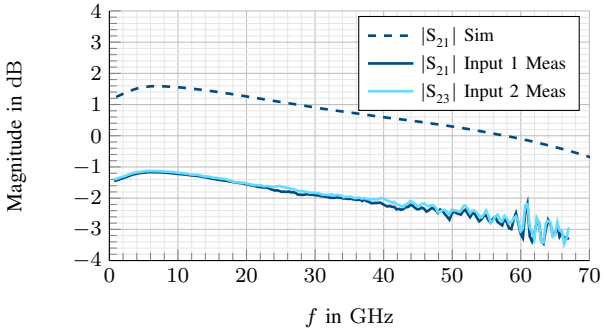

Fig. 7. Simulated and measured transmission of the transparent signal path.

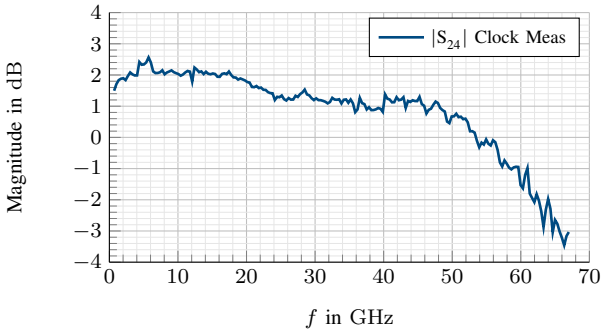

Fig. 8. Measured large signal transmission of the clock path for $P_{\text{in}} = 0\,\text{dBm}$.

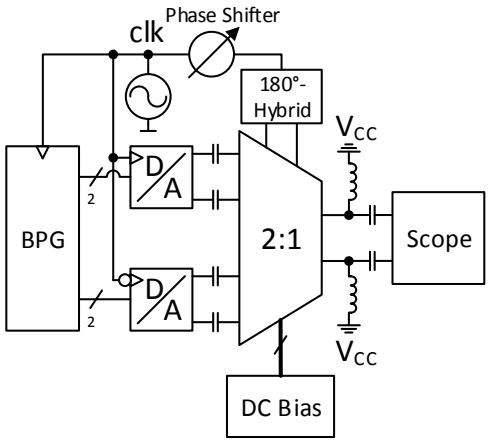

Fig. 9. Time domain measurement setup.

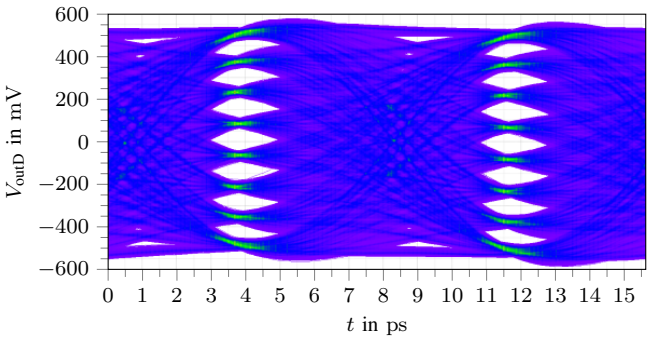

Fig. 10. Simulated PAM8 differential output signal V_{outD} at $128\,\mathrm{GS/s}$ aggregated sampling rate on post layout level.

AMUX, the timing relation between the DACs and the AMUX is adjustable via a phase shifter. The AMUX output signal is measured with a $70\,\mathrm{GHz}$ bandwidth sampling oscilloscope.

Simulations assuming the AMUX in an ideal measurement environment show open PAM8 eye diagrams at $128\,\mathrm{GS/s}$. Fig. 10 shows the corresponding eye diagram of the differential output voltage simulated with thermal noise.

First measurements with the setup depicted in Fig. 9 have been done without any digital pre-processing of the DAC input signals. Fig. 11 shows the resulting PAM4 eye diagrams of the single-ended measured outputs V_{out+} and V_{out-}. The single-ended peak-to-peak voltage swing is $375\,\mathrm{mV}$.

TABLE I gives a comparison of the measurement results to the key figures of other 2:1 analog multiplexers.

TABLE I
COMPARISON TO STATE OF THE ART

	Tech	P_{DC}	BW_{3dB}	f_s
[6]	InP	1.35 W	>40 GHz	50 GS/s[1]
[7]	InP	0.5 W	>50 GHz	100 GS/s
this work	SiGe	1.06 W	>67 GHz	>56 GS/s, 128 GS/s[1]

[1] Simulation only

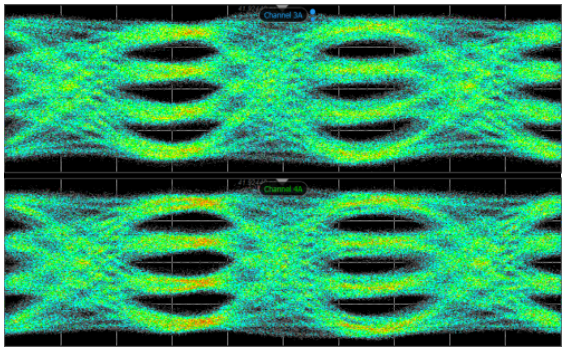

Fig. 11. Measured PAM4 output signals V_{out+} and V_{out-} at $56\,\mathrm{GS/s}$ aggregated sampling rate. Scale: $5\,\mathrm{ps/div}$, $55\,\mathrm{mV/div}$

IV. CONCLUSION

The presented 2:1 AMUX shows an excellent signal path 3-dB bandwidth exceeding $67\,\mathrm{GHz}$ which enables the generation of higher order modulation signals like PAM4 at very high sampling rates by time interleaving of two DACs. Measured open eye diagrams without any digital pre-processing have been shown for PAM4 at $56\,\mathrm{GS/s}$. This first measurements proof the potential of the presented AMUX. Measurements at higher sampling rates are under preparation. Time interleaving with an AMUX is a promising concept for high data rate signal generation.

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