This manuscript was presented at

2018 IEEE Nordic Circuits and Systems Conference (NORCAS), Tallin, Estonia, October 30-31, 2018.

A RF Pulse-Width and Pulse-Position Modulator IC in 28 nm FDSOI CMOS

Markus Grözing[1], Johannes Digel[1], Thomas Veigel[1], Robert Bieg[1], Jianxiong Zhang[1], Simon Brandl[1], Martin Schmidt[1], Christoph Haslach[2], Daniel Markert[2], Wolfgang Templ[2]
[1] Institute of Electrical and Optical Communications Engineering, University of Stuttgart, Germany
[2] Nokia Bell Labs, Stuttgart, Germany

***Abstract*— A pulse-width and pulse-position modulator (PWPM) IC for RF carriers from 170 MHz to 2.8 GHz is presented. The IC features a digital 5 bit pulse-width (PW) and 6 bit pulse-center (PC) input interface, updated at the RF carrier frequency, a small arithmetic unit, two delay locked loops with a new phase detector, two phase selectors, CMOS pulse logic and two differential binary RF outputs. At 900 MHz, a 14 MBd 256-QAM (112 Mb/s) signal with an EVM of 1.83 % and an ACLR of -45 dB is shown. At 2016 MHz, an ultra-broadband 504 MBd 16-QAM (2.016 Gb/s) signal with an EVM of 13.5 % and a BER of $1.5 \cdot 10^{-4}$ is demonstrated. The IC is implemented in a 28 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology and runs from a 1.0 V supply. It consumes 38 mW at 900 MHz and 58 mW at 2016 MHz carrier frequency.**

I. Introduction

The continuous growth of mobile data traffic and the increasing number of mobile standards and carrier frequencies imposes a challenge for the carrier frequency and bandwidth agility of future radio frequency (RF) transmitters. Furthermore, the RF power amplifiers (PA) have to provide non-constant-envelope signals with low error vector magnitude (EVM), a low adjacent channel power leakage ratio (ACLR) and high efficiency. Switched-mode power amplifiers (SMPA) [1] offer the potential to increase the efficiency compared to class AB PAs. RF transmitters supporting SMPAs need to supply one or several binary driver signals for the SMPA and a final reconstruction bandpass (BP) filter, as shown in Fig. 1. Suitable SMPA driver signals can be generated by a pulse-width and pulse-position modulator (PWPM) with digital baseband (BB) input that codes the amplitude and phase of the modulated signal into one or two (bipolar PWPM) binary signals [2, 3]. Aside from the final BP filter, the transmitter shown in Fig. 1 offers carrier frequency and bandwidth agility.

II. Modulator Concept

The block level schematic of the PWPM IC is shown in Fig. 2. A 64-phase (ϕ_0 to ϕ_{63}) carrier signal is generated from a supplied sine signal at f_C by a 73-stage delay line (DL) that is embedded into a delay locked loop (DLL) with a first phase detector and integrator ($\int PD(T_C)$). The DL has 5 precursor (ϕ_{-5} to ϕ_{-1}), 64 main cursor (ϕ_0 to ϕ_{63}) and 4 postcursor (ϕ_{64} to ϕ_{67}) stages. The delay between ϕ_{-1} (main DL input) and ϕ_{63} (main DL output) is regulated to one carrier period time $T_C = 1/f_C$ by the

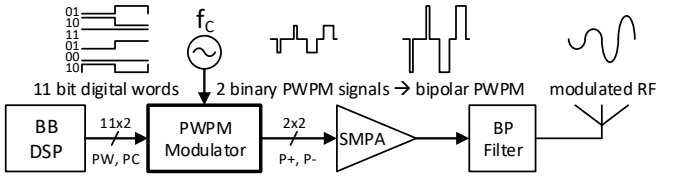

Fig. 1. RF transmitter with bipolar PWPM modulator, SMPA and bandpass reconstruction filter

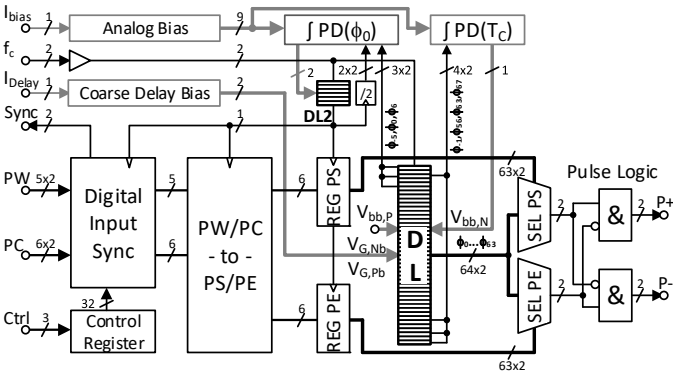

Fig. 2. RF PWPM IC block level schematic

DLL. The pre- and postcursor signal use is explained in section III.B. Two selectors (SEL) pick the phases for the rising and the falling edge of the final PWPM signal, controlled by 6 bit pulse start (PS) and pulse end (PE) control words. PE and PS are calculated by a small arithmetic unit from the 5 bit pulse-width (PW) and 6 bit pulse-center (PC) input words, updated at f_C.

Zero skew between the PE and PS signal word edges at the output of the registers (REG PS and PE) and the first output phase ϕ_0 of the main DL is ensured by clocking the registers by a second delay line (DL2) output. As the register output signal edge directions are random, a replica flip-flop is operated as a clock divider to get predictable alternating replica edges of the PS and PE signal edges at $f_C/2$. This replica edges are fed into a second phase detector ($\int PD(\Phi_0)$) to control DL2, employing an internal commutator for the replica edges alternating at $f_C/2$.

A 3-wire input control register and a digital input synchronization unit support the interfacing of the 11 bit digital input with high-speed transmitters of an FPGA. A final high-speed CMOS pulse logic generates two binary differential PWPM output signals (P+, P-) that can be combined – after amplification by two external SMPAs – to a single bipolar (levels -1, 0, +1) PWPM signal.

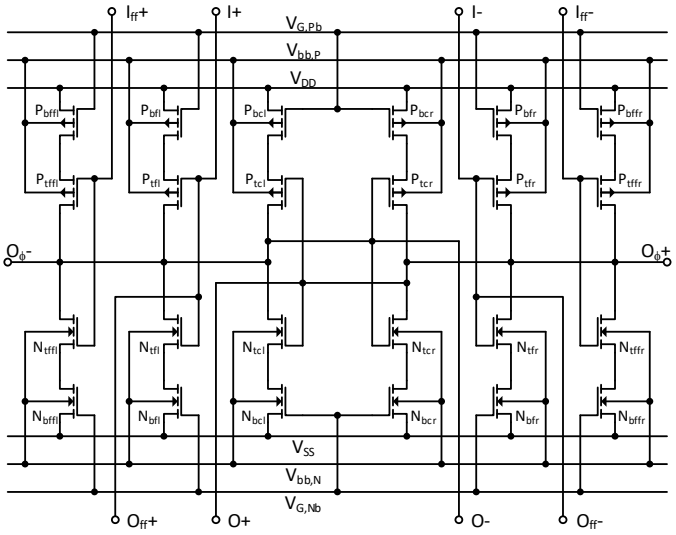

Fig. 3. Delay cell schematic

III. CIRCUIT DESIGN

A. Delay Cells and Delay Line

The delay cell shown in Fig. 3 uses a stacked static CMOS topology with stacked MOSFETs in both the pull-down and pull-up paths [4]. The upper p-channel- and the lower n-channel-MOSFETs act as current sources during switching and control the rise and fall times, respectively. Their gates are connected to a complementary coarse control voltage pair ($V_{G,Nb}$, $V_{G,Pb}$) that is generated from the coarse control input current (I_{Delay} in Fig. 2) via current mirrors and diode connected MOSFETs. Fine control of the delay time is implemented via the backgate voltage $V_{bb,N}$ of all FDSOI n-channel MOSFETs. The delay cell provides for full swing CMOS logic levels in any delay setting. The fully differential circuit topology with small cross-coupled inverters prevents any common mode signal buildup. The pins O_ϕ connect to the phase selectors SEL PS/PE.

Each delay cell interpolates between the output signals of two preceding delay cells. The current delay cell outputs O are connected to the inputs I of the following delay cell and the current delay cell outputs O_{ff} - which are directly connected to the preceding delay cell outputs O - are connected to the inputs I_{ff} of the following delay cell. Thus, additional feedforward paths bypassing one delay cell are established. This feedforward DL architecture allows for a minimum cell delay of about 5.6 ps at 1.0 V supply and thus for the generation of a 64-fold multiphase signal at 2.8 GHz carrier frequency.

B. Phase Detector and Integrator

A simplified schematic of the new analog current steering phase detector (PD) and following integrator is shown in Fig. 4. The phase detection is based on two complementary differential current steering switches (N_D and P_D) driven by the DL main section input ($S = \phi_{-1}$) and output ($E = \phi_{63}$) signals. The current source MOSFETs N_{SwCS} and P_{SwCS} must be biased active only during the rising edges of signals S+ and E+, otherwise rising and falling edge charges would compensate each other. This is implemented by MOSFETs N_{pre}, N_{post}, P_{pre} and P_{post} acting as voltage mode switches and controlled by DL signals that forego ($Pre = \phi_{56}$) and follow ($Post = \phi_{67}$) the DL output signal

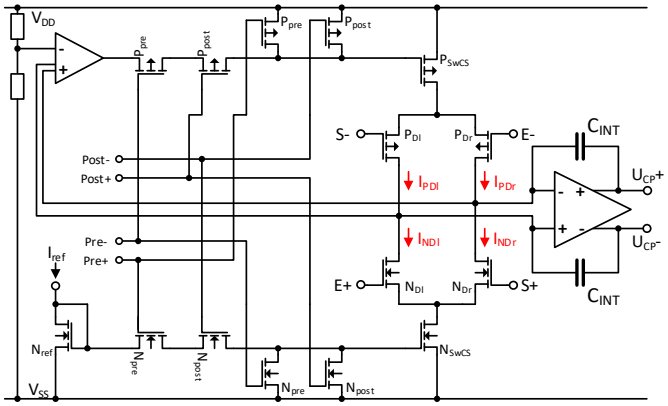

Fig. 4. Current steering phase detector and integrator schematic

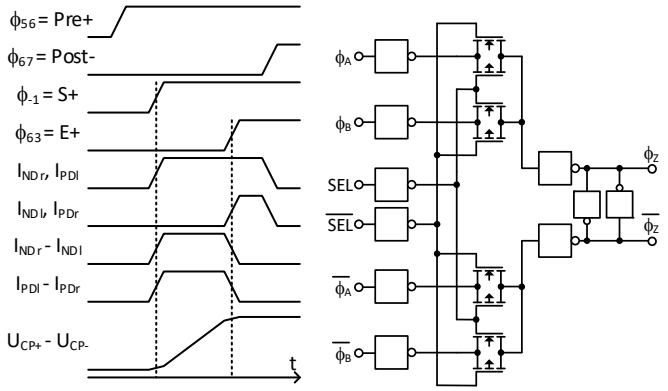

Fig. 5. (a) Phase detector signals (b) Basic 2:1 selector

($E = \phi_{63}$). To ensure proper operation of the current steering switches, the N_D and P_D drain common mode is regulated to $(V_{DD} + V_{SS})/2$ by a control loop controlling the source P_{SwCS}.

The transient operation of the PD and integrator for the rising S+ and E+ edges is shown in Fig. 5 (a). A phase difference, i.e. a time skew between the two differential input signals S and E, translates to differential output current pulses I_{NDr} - I_{NDl} and I_{PDl} - I_{PDr}. The current pulse charge is stored on the capacitors C_{INT} and translates to an output voltage difference $U_{CP+} - U_{CP-}$. This output voltage difference is converted to a single-ended signal and applied to the DL fine control input $V_{bb,N}$ (not shown in Fig. 4). The currents I_{NDr}, I_{NDl}, I_{PDl} and I_{PDr} stay switched off during the falling edges of S+ and E+.

As the PD does not include any regenerative flip-flop or latch circuitry, phase detection memory effects and hysteresis are avoided. Moreover, the PD output charge pulses disappear in delay lock, reducing the ripple on the DL control voltage as well as DLL jitter to a minimum.

C. Selectors and Pulse Logic

The two 64:1 selectors (SEL PS, SEL PE) are implemented as 6-level binary trees using 63 basic 2:1 selectors. The basic 2:1 selector shown in Fig. 5 (b) consists of static CMOS inverters for buffering and transfer gates for phase selection. All phase- (ϕ_A, ϕ_B) and selection- (SEL) -to-output (ϕ_Z) delay times are optimized for equal delay. Dummy buffers in the 64:1 selector tree delay the MSB selection signals to achieve a virtual phase selection at a single time instant. All signal paths are fully differential. The differential pulse logic uses static CMOS logic. Two input symmetric NAND and symmetric NOR gates [5] are used to implement the differential NAND function.

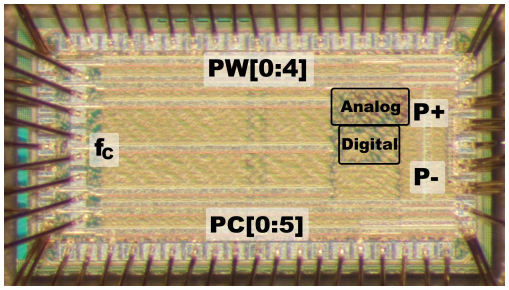

Fig. 6. RF PWPM IC photograph (chip area: 1.9 mm x 1.0 mm)

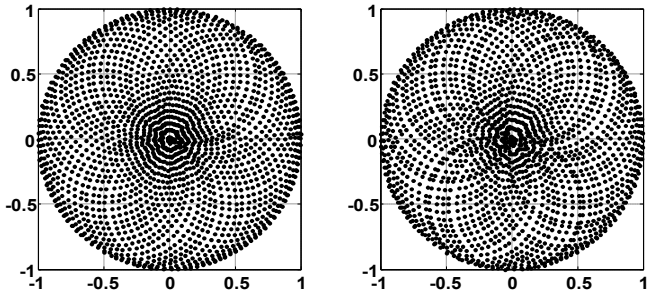

Fig. 7. Measured static output constellation diagrams for all PW&PC pulse patterns at 900 MHz (left) and 2016 MHz (right)

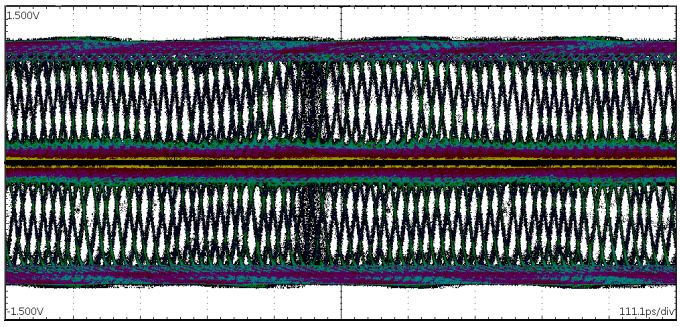

Fig. 8. Eye diagram of combined bipolar 64-phase output of the PWPM IC versus one carrier period at f_C = 900 MHz

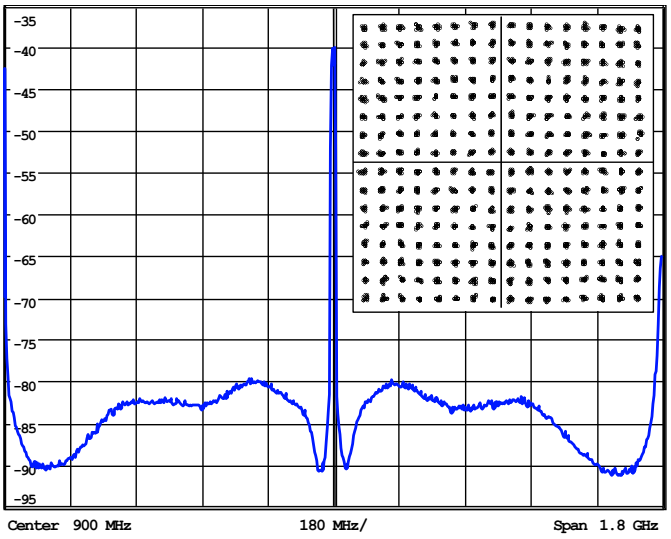

Fig. 9. Spectrum (RBW: 10 kHz, VBW: 1 MHz) and constellation of 14 MBd QAM-256 (112 Mb/s) signal at 900 MHz

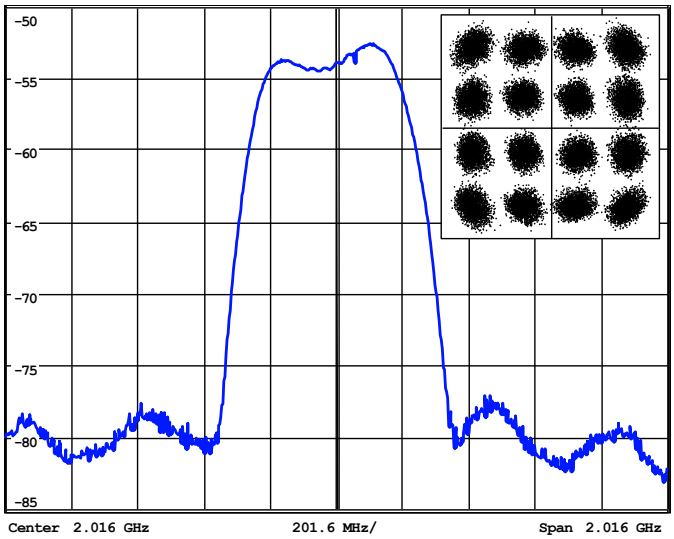

Fig. 10. Spectrum (RBW: 10 kHz, VBW: 1 MHz) and constellation of 504 MBd QAM-16 (2016 Mb/s) signal at 2016 MHz

IV. Experimental Results

Fig. 6 shows the photograph of the RF PWPM IC. The chip area is about 1.9 mm^2. The chip uses three 1.0 V supplies for the digital, analog and output driver circuitry. The carrier frequency f_C is supplied by a sine generator and the 11 digital inputs are connected to the GTH transmitters of a Virtex-7 FPGA on a VC7222 board. The four unipolar PWPM outputs are connected to a wideband oscilloscope for the time domain measurements. For the spectrum and narrowband constellation measurements with a vector signal analyzer, the four outputs are added by a tree of three broadband 180° hybrid couplers.

The delay line f_C tuning range for an externally applied coarse control current I_P between 0 µA and 950 µA is 169 MHz to 2.500 GHz at $V_{bb,P}$ = 0 V. When $V_{bb,P}$ is set to -1.0 V, f_C reaches 2.800 GHz. Thus the overall carrier frequency f_C tuning range is 169 MHz to 2.800 GHz.

A. Static Constellation Measurements

The 1985 different constellation points of the 2^{11} PW&PC combinations at 900 MHz and 2016 MHz carrier frequency are shown in Fig. 7. Each constellation point is measured by applying a constant PW&PC input word, capturing of the output signals with a wideband subsampling scope triggered by the carrier, and applying a DFT to the combined output signal. The constellations reflect effects of static delay time mismatches of the delay cells and the signal paths in the selectors, as well as the limited bandwidth of the pulse logic and output drivers.

B. Offline Preprocessing

Offline preprocessing is used to generate the PW and PC input data for the PWPM. The used procedure is similar to [6]: A complex quantizer encodes the upsampled baseband IQ sequence into a PW&PC sample sequence. The quantizer mapping is done with the measured constellations (Fig. 7). The quantizer chooses the PW&PC point closest to the actual input IQ sample. The remaining quantization error between the quantizer input and output is fed to a digital ΔΣ feedback loop to obtain noise shaping near the carrier frequency.

TABLE I
SUMMARY OF MEASURMENT RESULTS

Property	Unit	1	2	3	4	5
Carrier freq.	MHz	900	2016	2016	2016	2016
Symbol rate	MBd	14.06	15.75	31.50	63.00	504.0
Modulation	QAM	256	256	256	64	16
Data rate	Mb/s	112.5	126.0	252.0	378.0	2016
EVM	%	1.83	2.36	2.47	3.97	13.5
SNDR	dB	34.7	32.5	32.1	28.0	17.4
BER *		$< 10^{-8}$	$1 \cdot 10^{-6}$	$3 \cdot 10^{-6}$	$1 \cdot 10^{-8}$	$1.5 \cdot 10^{-4}$ **
Ch. BW	MHz	18.0	22.5	45.0	90.0	720
Ch. spacing	MHz	20.0	25.0	50.0	100.0	800
BW efficiency	b/Hz	6.22	5.6	5.6	4.2	2.8
$ACLR1_{,Lower}$	dB	-44.8	-42.9	-42.2 /	-38.4	-24.7
$ACLR1_{,Upper}$	dB	-44.8	-41.8	-40.7	-36.1	-25.1
$ACLR2_{,Lower}$	dB	-49.2	-49.0	-45.7 /	-36.1	-20.1
$ACLR2_{,Upper}$	dB	-48.6	-47.1	-43.6	-37.3	-23.7

*) estimated [7] **) measured

TABLE II
COMPARISON TO THE STATE-OF-THE-ART

Property	Unit	[8]	[9]	[10]	[11]	This Work
CMOS techn.	nm	32	40	45	28	28
Carrier frequency range	GHz	2.4	0.9 - 2.6	1.0 - 3.0	0.35 - 2.6	0.17 - 2.8
max. signal BW[1]	MHz	40	40	N/A	400	504
Binary outputs		yes	yes	yes	no	yes
Carrier freq.	MHz	2400	2000	2400	2000	2016
DC power	mW	82	91	35	670	58
Signal type		WLAN	WLAN	GMSK	OFDM	SC RC[2]
QAM order		64	64	4	64	256
Data rate	Mb/s	54	54	20	120	126
Bandwidth	MHz	20	20	N/A	20	22.5
EVM	dB	-32	-29	-33.5	-29	-32.5
PAPR	dB	N/A	8[3]	0	8	6.5
ACLR1	dBc	N/A	-30[3]	N/A	-40	-42

[1]) demonstr. by experiment [2]) single carrier raised cosine with $\beta = 0.5$
[3]) 20 MHz BW DMT signal

C. Modulated RF Signal Measurements

Upsampled single carrier (SC) quadrature amplitude modulated (QAM) raised cosine (RC) filtered signals are used to demonstrate the capabilities of the PWPM IC. A spectrum and vector signal analyzer and a broadband 80 GS/s 20 GHz real-time scope are used to characterize the RF output signal quality. Fig. 8 shows the eye diagram of a combined bipolar 14 MBd 256-QAM output signal at 900 MHz versus one carrier period. The bipolar levels and the 64 phase quantization of the combined output are clearly visible. Fig. 9 shows the corresponding spurious-free far-out spectrum and the constellation diagram of the modulated RF output signal. The signal shows an adjacent ACLR of -44.8 dB and an EVM of 1.83 %. The EVM corresponds to an estimated bit error rate (BER) smaller than 10^{-8} for the 112 Mb/s signal [7]. The code efficiency of the PWPM signal is the ratio of the fundamental signal power around f_C to the overall signal power including the harmonics at $n \cdot f_C$, $n > 1$. By measuring the 1st to 8th harmonic powers, the code efficiency at 900 MHz is estimated to 75 %. Fig. 10 shows the spectrum and the constellation diagram of an ultra-broadband 504 MBd 16-QAM signal at 2016 MHz carrier. The measured EVM and BER of the 2016 Mb/s RF signal are 13.5 % and $1.5 \cdot 10^{-4}$, respectively. Table I summarizes the measurements at 900 MHz and 2016 MHz carrier with various bandwidths and QAM orders.

V. CONCLUSION

The comparison to other state-of-the-art digital phase and pulse-width modulators with carrier frequencies at around 2 GHz is shown in Table II. This work offers the RF output signal with the largest instantaneous bandwidth (504 MHz), with the highest QAM order (QAM-256), and a 22.5 MHz bandwidth output signal with the best EVM for non-constant-envelope (PAPR = 6.5 dB) modulation. Moreover, a clean far-out spectrum and a good code efficiency is shown. This performance is enabled by using a new hysteresis-free phase detector circuit, by applying static digital predistortion in combination with delta-sigma-modulation and by a frequent update of the PW&PC samples at the carrier frequency rate.

As an outlook to real-time operation, the digital preprocessing, done offline so far, may be integrated with the modulator on a future single IC. As an outlook to the support of higher carrier frequencies, the delay line length may be cut back. The resulting phase resolution loss can be compensated by either phase interpolation or by the larger oversampling ratio that is available at higher carrier-frequency-to-bandwidth ratios.

REFERENCES

[1] S. Heck, M. Schmidt, A. Bräckle, F. Schuller, M. Grözing, M. Berroth, H. Gustat, and C. Scheytt, "A switching-mode amplifier for class-S transmitters for clock frequencies up to 7.5 GHz in 0.25µm SiGe-BiCMOS", *in RFIC 2010,* Anaheim, CA, 2010.

[2] F. Raab, "Radio Frequency Pulsewidth Modulation", *IEEE Trans. Commun,* vol. 21, no. 8, pp. 958–966, 1973.

[3] J. S. Walling, H. Lakdawala, Y. Palaskas, A. Ravi, O. Degani, K. Soumyanath, and D. J. Allstot, "A Class-E PA With Pulse-Width and Pulse-Position Modulation in 65 nm CMOS", *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1668–1678, 2009.

[4] M. Grözing, B. Phillip, and M. Berroth, "CMOS ring oscillator with quadrature outputs and 100 MHz to 3.5 GHz tuning range," in *ESSCIRC 2003,* Estoril, Portugal, 2003.

[5] J. Digel, M. Grözing, M. Schmidt, M. Berroth, and C. Haslach, "Digital pulse-width pulse-position modulator in 28 nm CMOS for carrier frequencies up to 1 GHz", *in RFIC 2015,* Phoenix, AZ, USA, 2015.

[6] D. Markert, X. Yu, H. Heimpel, and G. Fischer, "An All-Digital, Single-Bit RF Transmitter for Massive MIMO", *IEEE Trans. Circuits Syst. I*, vol. 64, no. 3, pp. 696–704, 2017.

[7] A. Svensson, "An Introduction to Adaptive QAM Modulation Schemes for Known and Predicted Channels", *Proc. IEEE*, vol. 95, no. 12, pp. 2322–2336, 2007.

[8] P. Madoglio, A. Ravi, H. Xu, K. Chandrashekar, M. Verhelst, S. Pellerano, L. Cuellar, M. Aguirre, M. Sajadieh, O. Degani, H. Lakdawala, and Y. Palaskas, "A 20dBm 2.4GHz digital outphasing transmitter for WLAN application in 32nm CMOS", *in ISSCC 2012,* San Francisco, CA, USA, 2012.

[9] S. Kulkarni, I. Kazi, D. Seebacher, P. Singerl, F. Dielacher, W. Dehaene, and P. Reynaert, "Multi-standard wideband OFDM RF-PWM transmitter in 40nm CMOS", *in ESSCIRC 2015,* Graz, Austria, 2015.

[10] H. Gheidi, T. Nakatani, V. W. Leung, and P. M. Asbeck, "A 1–3 GHz Delta–Sigma-Based Closed-Loop Fully Digital Phase Modulator in 45-nm CMOS SOI", *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1185–1195, 2017.

[11] M. Kosunen, J. Lemberg, M. Martelius, E. Roverato, T. Nieminen, M. Englund, K. Stadius, L. Anttila, J. Pallonen, M. Valkama, and J. Ryynanen, "13.5 A 0.35-to-2.6GHz multilevel outphasing transmitter with a digital interpolating phase modulator enabling up to 400MHz instantaneous bandwidth", *in ISSCC 2017,* San Francisco, CA, USA, 2017.