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64-GS/s 6-bit Track-and-Hold Circuit With More Than 61 GHz Bandwidth at 1.0 V_{pp} Input Voltage Swing in 90-nm SiGe BiCMOS Technology

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***Abstract*—Time-interleaving of energy-efficient data converter cores enables record symbol rates in electronic receivers. High-speed applications like optical data transmission or direct down-conversion in wireless mmWave receivers require ultra-high bandwidths and symbol rates, which CMOS data converters and especially their analog front ends cannot provide to date. We demonstrate a 64-GS/s track-and-hold circuit with a large-signal bandwidth of more than 61 GHz without any area-consuming peaking inductors, designed and manufactured in a 90-nm SiGe BiCMOS technology. The analog sampling front end exhibits a third harmonic distortion of -45 dBc to -32 dBc within the available frequency range of 50 GHz, which is better than the 5-bit requirement for 1.0-V_{pp} input signals. The ultra-high bandwidth of the circuit is twice as high as reported for CMOS data converters and in the range of broadband germanium photodiodes. This improves the bottleneck in hybrid integrated optoelectronic receiver front ends significantly. It is suited for time-interleaving of two channels with a doubled symbol rate of 128 GBaud, and the linearity allows to use it with 6–8-bit data converters.**

Keywords—analog-to-digital conversion, bicmos integrated circuits, sampled data circuits, silicon-germanium, switched emitter follower, track-and-hold circuit.

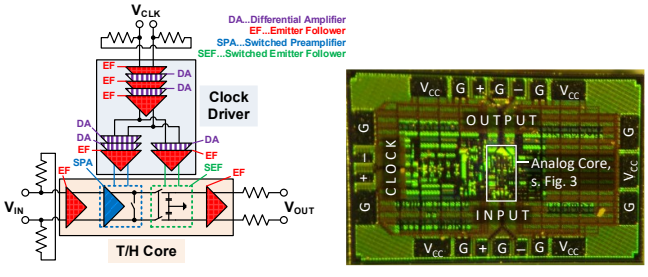
I. Introduction

Electrical bandwidth is an ever more important feature in emerging communication systems. In the mobile sector, the 5G mmWave spectrum becomes available and enables the multi-Gbit/s range for cellular clients, empowering ultra-high definition video streaming, and augmented and virtual reality. Vehicles and infrastructure start to communicate and develop intelligent traffic routing, parking lot management and autonomous driving. Although omnidirectional base stations give way to smaller cells with directional beamforming, the sheer amount of aggregated data requires fiber-optical data links for exchange with service providers and data centers. Various wavelengths are multiplexed onto single fibers to process the data traffic with low latency close to where they are needed. Most commonly, germanium photodiodes and transimpedance amplifiers convert the optical information back into an analog electrical signal in the receiver, with a bandwidth of 50–70 GHz. The subsequent data converter stage represents the bottleneck in ultra-wideband data transmission because state-of-the-art ADCs provide bandwidths of typically around 30 GHz or below [1]. Sampling front ends in InP technology often reach higher bandwidths but are expensive and more difficult to integrate than silicon solutions, which is important to reduce module costs towards 1 $ per Gbit.

SiGe BiCMOS technologies represent efficient ways for the utilization of ultra-fast bipolar transistors and partial integration of digital processing, especially in CMOS nodes below 100 nm. We present a track-and-hold circuit in such a state-of-the-art 90-nm SiGe BiCMOS technology. The circuit is designed to deliver a sufficient bandwidth for directly converting the second Nyquist band into the baseband without any significant attenuation, which has several advantages like simple low-pass filtering of harmonics at the input stage, or the absence of an additional mixer stage and local oscillator. In an optical receiver, the presented track-and-hold circuit can be used to process ultra-high symbol rates with a reduced data converter bandwidth, when a 2-channel time-interleaving scheme is applied, e.g. 128 GBaud with 64 GHz bandwidth at the input and two 64-GS/s ADCs with 32 GHz bandwidth connected to the time-interleaved track-and-hold circuit's outputs. This is feasible for state-of-the-art CMOS data converters, which shows how SiGe bipolar transistors and CMOS can coexist and exhibit synergy effects rather than replacing each other in today's ultra-wideband communication systems.

II. Circuit Architecture

Fig. 1 shows the realized track-and-hold circuit. A switched emitter follower (SEF) samples the input voltage in track mode and stores it on a hold capacitor during hold mode, with low loss and distortion. The hold mode signal quality is preserved by a high input impedance output buffer and by the switched preamplifier (SPA) that is silenced during hold mode. Differential amplifier stages steepen the edges of the clock signal, with one of them acting as a delay element for the SPA, and intermediate emitter follower buffers provide driving capability and level shifting. This architecture has shown valuable results, ranging from a 6.4-GS/s [2] and a 12.8-GS/s [3] chip for radar applications to a 32-GS/s circuit with 58-GHz bandwidth in [4]. Emitter follower buffers facilitate input and output matching with a differential 100 Ω resistance, as they exhibit a high input impedance, as well as a low output impedance around 5 Ω.



(a) (b)

Fig. 1. (a) Block diagram and (b) chip microphotograph of the track-and-hold circuit with pad-limited dimensions of 1.5 mm x 1.0 mm.

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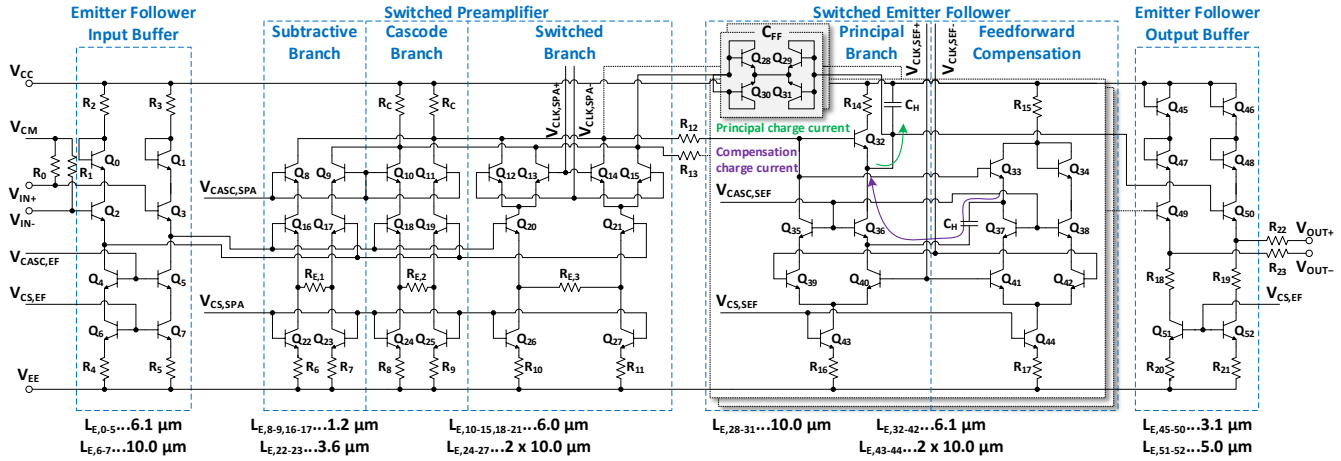

Fig. 2. Schematic of the track-and-hold circuit's analog core with subtractive linearization in the switched preamplifier, feedforward compensation in the switched emitter follower, and emitter follower input and output buffers. Emitter lengths are provided for each stage.

In this work, we demonstrate a further performance increase of this inductor-less architecture. With the circuit topology of the analog core in Fig. 2 and by using a high-performance Infineon Technologies 90-nm SiGe BiCMOS process, we increase the sampling rate to 64 GS/s and maintain an ultra-high bandwidth and a linearity suitable for 6–8-bit data converters with 1-V_{pp} differential input voltage swing. The oscillation tendency of cascaded emitter follower stages, in particular with more than two, increases with faster transistor transit frequencies. Hence, we omit the second emitter follower output buffer in the track-and-hold core in comparison with other implementations. The SPA and SEF are linearized with subtractive gain composition and feedforward compensation, respectively, as in [4]. The subtractive branch increases the linear input range and the bandwidth of the SPA at the cost of a slightly reduced gain. The feedforward compensation maintains a low harmonic distortion of the SEF at high input frequencies. This is achieved by injecting the necessary current to charge the hold capacitance into the principal branch, stabilizing the base-emitter voltage of Q_{32} in track mode at the cost of increased power consumption. Output termination resistors R_{22-23} are added for matching the output to the 50-Ω measurement environment. The series-connection attenuates the output signal by -6 dB and can be omitted in a monolithically integrated data converter IC or in a hybrid integration, if 50-Ω matching is not necessary.

For mmWave frequencies, a compact symmetrical IC layout is crucial to avoid unwanted effects in differential circuits, e.g. from thermal distribution or layout parasitics mismatch. The IC core layout shown in Fig. 3 was designed with these special requirements in mind. The largest resistor R_C between the SPA and the SEF carries the largest average current and is a potential hot spot. The placement in the middle of the analog core is meant to help distribute heat evenly to the subcomponents. Many symmetry axes can be found across the chip to maintain signal integrity of the differential signals. At the inputs and outputs, both signals are routed adjacently in custom designed differential 100-Ω transmission lines on the highest copper layer, which were modelled using the 2.5-D EM simulator Momentum. The technology utilized in this work provides high-performance heterojunction bipolar transistors with 300-GHz transit frequency and 480-GHz maximum oscillation frequency. A micrograph of the manufactured chip is depicted in Fig. 1 (b).

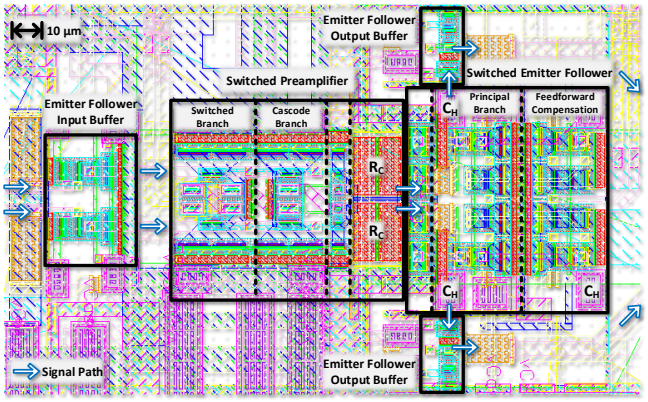

Fig. 3. Layout of the analog core with indicated subcomponents and signal path directions on an overall silicon area of 0.023 mm².

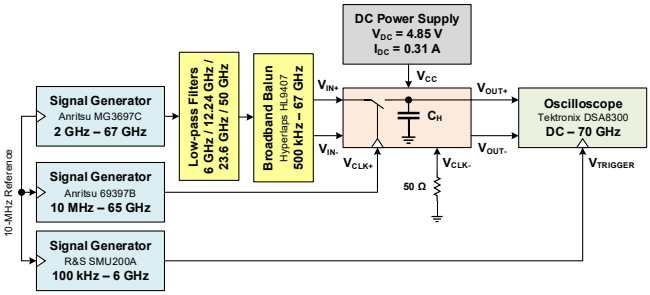

Fig. 4. Measurement setup with a sub-sampling oscilloscope, DC blocks at the RF probes are not shown.

III. Experimental Results

For performance evaluation, the IC was glued with thermal adhesive to a copper coin, in order to spread the dissipated heat, and contacted with a wafer prober station through 67-GHz and 40-GHz GSGSG-probes (with additional power pins) for the differential input and output signals, respectively, and a 20-GHz GSSG-probe for the differential clock signal. The clock path suffers from a large attenuation by the measurement environment, which decreases the achievable signal-to-noise ratio. Yet, the clock driver is sensitive enough to be able to show sampling at 64 GS/s.

Fig. 4 illustrates the measurement setup. The signal generator's output amplitude was maintained at a constant level, and the attenuations of low-pass filters, cables and broadband balun were determined with a sampling

oscilloscope within the available frequency range. The signal generator's output amplitude was adjusted by the calculated losses and verified, until the output amplitude showed only marginal differences from the desired 1 V_{pp}, with no less than -0.2 dB at the highest possible signal frequency of 61 GHz (without filters). At higher input frequencies, the signal generator would be unleveled. The attenuation of output cables and probe-tips was measured and subtracted from the chip's signal path attenuation for frequencies up to the Nyquist frequency of 32 GHz, higher spectral components were mirrored into the first Nyquist band and considered with their alias frequencies. The track-and-hold circuit's frequency response was determined with a full 64-GS/s sampling rate to demonstrate the large-signal bandwidth of the chip. The sub-sampling oscilloscope captured 64 averaged samples of the output signal with a 70-GHz differential sampling module.

Fig. 5 shows the transient output signal for a 61-GHz sinewave with 1-V_{pp} differential amplitude applied at the input of the circuit, whilst being operated at 64 GS/s. One point per hold interval was processed using an FFT with a total of 128 points, as indicated. The resulting frequency spectrum is plotted in Fig. 6. Low-pass filters were used up to 50 GHz, to attenuate the 2nd harmonic of the signal generator. The 3rd harmonic distortion HD3, which is especially harmful in multi-tone applications as a third-order intermodulation product, is depicted in Fig. 7. The mean values for 10 measurements are given in this picture. The HD3 ranges between -45 dBc and -40 dBc up to 22 GHz, indicating an equivalent max. accuracy of more than 6 bits. Up to 50 GHz, the HD3 stays below the 5-bit threshold of -32 dBc, indicating the potential of an integration with a 6-bit analog-to-digital converter. The total harmonic distortion (THD) is better than -32 dB up to 22 GHz, but shows a strong increase with the 50 GHz low-pass filter, by approximately 1 bit, just as the HD3. Weak synchronization between the signal, clock, and trigger generator becomes more visible at these higher frequencies, and the THD and HD3 curves follow the reference path.

The frequency response in Fig. 8 is normalized with respect to the maximum expected output signal level and takes the resistive voltage divider at the output into account. It shows that the attenuation of the sampled signal path at the highest available signal frequency of 61 GHz for 1.0 V_{pp} is still less than -3 dB below the maximum for the first Nyquist band at 64 GS/s. This indicates a 3 dB-bandwidth beyond 61 GHz, enabling reception of mmWave radio channels without a down-converter. Furthermore, it demonstrates that 2-fold time-interleaving is suitable, which would allow to receive 128 GBaud with a 32-GHz bandwidth requirement for the two interleaved ADCs.

The performance values are summarized in Table I and compared with state-of-the-art track-and-hold circuits with an ultra-high bandwidth and sampling rate. Compared with [4], this implementation achieves double the sampling rate, a higher bandwidth and a max. HD3 value that is by 3 dB better for the same input voltage swing. With the advanced technology and an adapted architecture, the power consumption of the analog core could be reduced by a third, and its active area by a half. The circuit in [5] with a comparable SiGe technology uses the SEF as well, but no preamplifier, resulting in a slightly higher bandwidth, but lower sampling rate, input voltage swing and linear frequency range with a comparable DC power dissipation in the analog core. For sampling front ends above 40 GS/s, the presented track-and-hold circuit exhibits the highest bandwidth. The difference in comparison with the ICs in [6] and [7] is 10 GHz and 20 GHz, respectively. It must be emphasized though that the latter consumes significantly less power, thanks to a combination of MOS and HBT devices optimized for low-power operation. In addition, it is the only comparable IC that can beat the small footprint of the presented track-and-hold circuit. Further bandwidth improvement with integrated peaking inductors and reduction in power consumption by means of passive and low-power clock driver components can be addressed in future research.

IV. Conclusion

A track-and-hold circuit with more than 61 GHz bandwidth at 64 GS/s and a 1.0 V_{pp} differential input voltage swing was designed and manufactured in a pre-production 90-nm SiGe BiCMOS technology. The careful design and layout of the circuit including linearization techniques for the SPA and the SEF, together with the ultra-high transistor switching speed, permit the demonstration of the highest bandwidth for reported sampling circuits above 40 GS/s. Without the use of any space-consuming peaking inductors, the analog core circuitry only requires a footprint of 0.023 mm² in the layout.

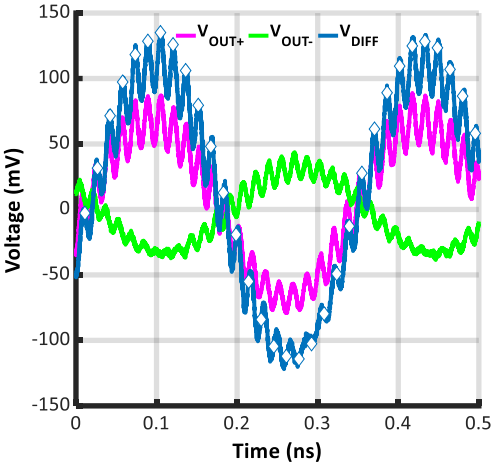

Fig. 5. Time-domain plot of the averaged output signal for a 61-GHz 1.0-V_{pp} sinusoidal input, sampled at 64 GS/s. Sampling instants are indicated by white diamonds.

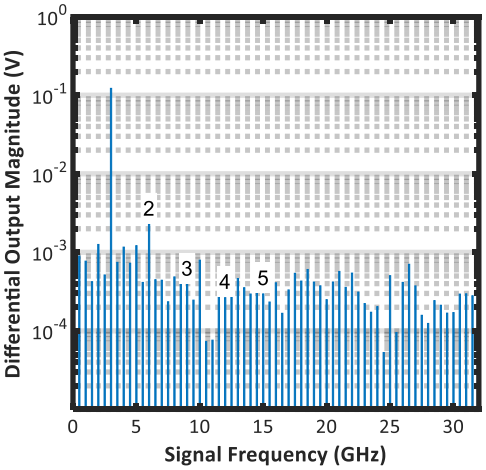

Fig. 6. Frequency spectrum for a 61-GHz 1.0-V_{pp} sinusoidal input with 64 averages, 128-point FFT (one point per hold interval). The second harmonic of the signal generator is dominant due to the high input signal level, other harmonics are within the noise floor.

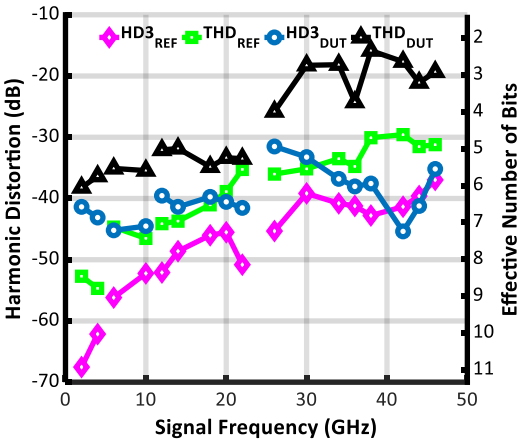

Fig. 7. Third harmonic distortion (HD3) and total harmonic distortion (THD) of the reference path (REF) and the averaged output signal (DUT), across the available frequency range of low-pass filters for a 1.0-V_{pp} differential input signal, sampled at 64 GS/s.

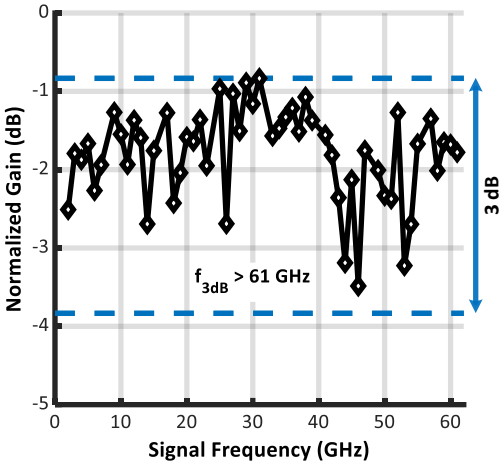

Fig. 8. Frequency response with compensated measurement setup losses, operating at 64 GS/s and 1.0 V_{pp} input voltage swing. The gain is normalized with respect to a 500-mV_{pp} output amplitude due to the resistive voltage divider with the 50 Ω measurement equipment.

The ultra-high bandwidth approaches the one of germanium photodiodes, significantly improving the analog electronics front end in the optical receiver, which is important for high-speed data transport in fiber-optical links. With an HD3 below the 5-bit threshold, the circuit can be used for data converters with 6–8 bits. Modulation formats beyond PAM-4 at 64 GBaud in high-speed optical modules may be possible to achieve with the presented analog front end. With a 2-fold time-interleaving, the symbol rate could be further increased to 128 GBaud. The circuit also provides a way for converting mmWave frequencies above 32 GHz down into the baseband without any additional mixer stage, for direct conversion in 5G mmWave base stations. In a massive MIMO receiver, up to 64 channels with 400-MHz bandwidth and 100-MHz spacing on a radio carrier in the first or second Nyquist band could be covered simultaneously.

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TABLE I. COMPARISON OF TRACK-AND-HOLD CIRCUITS WITH ULTRA-HIGH BANDWIDTH AND SAMPLING RATE.

Ref.	Sampling Rate	Bandwidth	Third Harmonic Distortion	Diff. Input Voltage Swing	Total / Core Power Consumption	Total / Core Active Area	Technology f_T / f_{max}
[4]	32 GS/s	58 GHz (large-signal)	-64 dBc to -29 dBc (2 – 61 GHz)	1.0 V_{pp}	1.8 W / 685 mW	1.5 / 0.044 mm²	130-nm SiGe 250 / 400 GHz
[5]	40 GS/s	70 GHz	-48 dBc to -32 dBc (1–19 GHz)	0.45 V_{pp}	— / 440 mW	0.72 / 0.046 mm²	130-nm SiGe 300 / 500 GHz
[6]	70 GS/s / 60 GS/s [1]	51 GHz	-52 dBc to -37 dBc (0–15 GHz)	0.4 V_{pp}	1.9 W / —	1.8 mm² / —	700-nm InP 320 GHz / —
[7]	108 GS/s / 90 GS/s [2]	40 GHz	-44 dBc to -34 dBc (20 & 40 GHz)	0.4 V_{pp}	0.09 W / 20 mW	0.489 / 0.018 mm²	55-nm SiGe 330 / 350 GHz
This Work	**64 GS/s**	**>61 GHz (large-signal)**	**-45 dBc to -32 dBc (2 – 50 GHz)**	**1.0 V_{pp}**	**1.5 W / 465 mW**	**1.5 / 0.023 mm²**	**90-nm SiGe 300 / 480 GHz**

[1] Max. sampling rate 70 GS/s, linearity measured at 60 GS/s. [2] Max. sampling rate 108 GS/s, linearity measured at 90 GS/s.