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Analog 2:1 Multiplexer with over 110 GHz Bandwidth in SiGe BiCMOS Technology

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***Abstract*—We report on a 2:1 analog multiplexer (AMUX) circuit in 130-nm SiGe BiCMOS technology. The technology offers HBTs with peak f_T of 470 GHz and f_{max} of 650 GHz. S-parameter measurements of the AMUX IC show a significant leap in bandwidth compared to the circuit in the previous technology generation. The linear signal path offers a 3-dB-bandwith beyond 110 GHz, while the limiting clock path has 85 GHz 3-dB-bandwidth. With this circuit two digital-to-analog converters (DACs) can be time-interleaved, to generate multi-level signals far beyond 100 GBaud with both high bandwidth and linearity.**

Keywords— analog multiplexer (AMUX), silicon-germanium (SiGe), heterojunction bipolar transistor (HBT), time interleaving, digital-to-analog conversion, multiplexing

I. Introduction

In high data rate communication systems, the analog bandwidth of data converters is a major limiting factor to be overcome. On the transmitter side, the bandwidth of widely used CMOS digital-to-analog converters (DACs) seems to approach a limit, as the analog performance of upcoming CMOS technology nodes is not expected to improve substantially [1]. As a viable response to this problem, the interleaving of several converters using additional front-end circuits in bipolar technology is discussed [1]-[3]. Synchronous time-interleaving of DACs with an analog multiplexer (AMUX) is a promising approach among other bandwidth enhancement techniques. With the AMUX, sampling rate and bandwidth of multiple DACs are aggregated. However, this comes at the cost of increased power consumption and high linearity requirements for the AMUX in order to prevent degradation of the overall linearity.

In the field of analog multiplexers, circuits in SiGe [4]-[6] as well as InP [3],[7]-[9] technologies have been demonstrated. Circuits in InP show signal path and clock path bandwidths over 110 GHz, enabling signal generation up to 168 GBaud with four levels (PAM4) [8]. SiGe circuits stay a bit behind in performance with demonstrated 120 GBaud PAM4 signals with 50 GHz signal path and 64 GHz clock path bandwidth [6]. However, SiGe technology is better suited for large scale commercialization due to the mature silicon processes with good yield and low costs, also allowing for more complex circuits than InP. With recent progress in SiGe technology, the performance gap to InP is further decreased.

The AMUX circuit presented in this paper uses the same topology as the circuit presented in [4]. The two AMUX circuits are implemented in two generations of IHP's 130-nm BiCMOS technology, which differ in RF performance of the SiGe HBTs. The first design [4] is implemented in the technology SG13G2 [10]. The second circuit – presented in this paper – is implemented in a development variant of a new process generation called SG13G3. This SiGe technology advancement enables the demonstration of a significant bandwidth leap, increasing the signal path bandwidth to over 110 GHz.

In section II we show the advances of the used SiGe technology, section III gives an overview of the circuit design, the S-parameter measurements are presented in section IV and section V concludes the paper.

II. Technology

The technology SG13G2 [10] – in which the first circuit is designed – provides SiGe HBTs with peak f_T values of 350 GHz and peak f_{MAX} values of 450 GHz. Main features of the presented circuit's new HBT technology generation SG13G3 and transistor optimization for high speed are outlined in [11]. The HBT models used for the current designs are extracted from HBTs with peak f_T/f_{MAX} values of 470 GHz/610 GHz corresponding to an early development stage of the BiCMOS

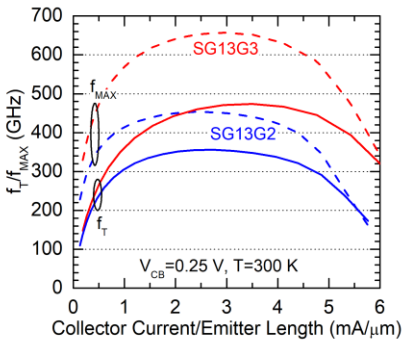

Fig. 1. Measured f_T and f_{MAX} as a function of collector current per emitter length for both technologies. Devices with eight emitters of 1 µm length in parallel were measured. The emitter width is 130 nm for the SG13G2 device and 110 nm for the SG13G3 device.

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process [12]. The HBTs of the present fabrication feature the same f_T values (470 GHz) and slightly higher f_{MAX} values of about 650 GHz as extrapolated from the unilateral power gain at frequencies around 20 GHz with an ideal slope of -20 dB/decade (Fig. 1).

Both BiCMOS technologies feature the same 130 nm CMOS process and an equivalent suite of passive devices. The dual-gate-oxide CMOS process provides 1.2 V core and 3.3 V I/O devices. Passive elements include salicided and unsalicided poly-silicon resistors, silicon nitride MIM capacitors, and MOS varactors. Due to the smaller unsalicided poly-silicon resistor sheet resistance of the latest technology, the presented circuit with same resistor geometries as the former one features slightly higher currents and offers more gain. The metallization consists of seven aluminum layers including five fine-structured layers and two thick top metal layers with 2 µm and 3 µm thickness for transmission lines, inductors, and transformers.

III. Circuit Design

A block diagram of the AMUX circuit and chip photograph are given in Fig. 2. All inputs and outputs are differential with 100 Ω termination. The AMUX core is driven by a multi-stage limiting clock amplifier with adjustable duty cycle, to omit duty cycle error impairments. One of the two inputs is selected by the clock signal and forwarded to the output. An additional output amplifier drives the external differential 100 Ω load.

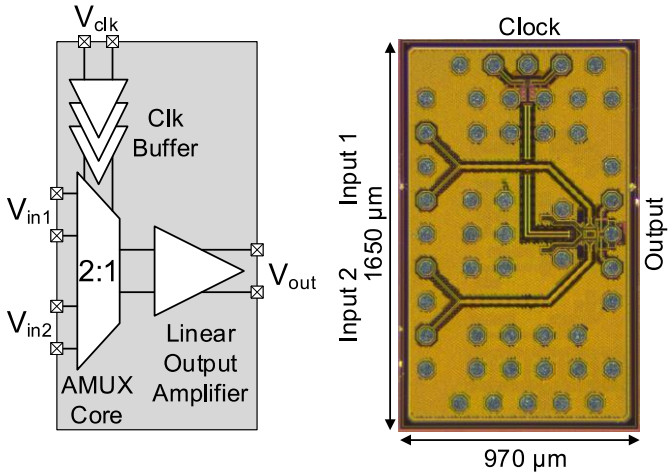

Fig. 2. AMUX block diagram and chip photograph.

Fig. 3 shows the schematic of the AMUX core and output amplifier. The core consists of a linearized Gilbert-cell for each input, with outputs connected in parallel. Depending on the state of the clock signal, the output current of the active input cell is switched to the common output, comprising cascode transistors and load resistors, whereas the current of the inactive cell is switched to a dummy path. The inputs of the Gilbert-cells are preceded by 100 Ω resistive termination (not shown) and emitter followers. The output amplifier consists of two emitter followers and a linearized differential amplifier with cascode output. The internal load resistors $R_{L,out}$ of 50 Ω provide good matching at least for low frequencies. DC current for the differential amplifier is provided by external bias tees, so the internal load resistors are only subject to the AC part, which allows for resistors with smaller area and less parasitic capacitance.

The AMUX core's voltage gain is only about 0.53, smaller than 1. The voltage gain of the core is intentionally traded in for more bandwidth. Furthermore less voltage swing in the core allows for less DC and AC current (for a given load resistor) and smaller transistors, which in turn leads to smaller parasitics. Therefore, the clock driver has to drive a smaller capacitive load. The output amplifier provides a voltage gain of about 2.7. The signal path from input to output has simulated voltage gain of 1.4, corresponding to 3 dB.

The static transfer function for differential DC voltages is given in Fig. 4, simulated including parasitic resistance. High linearity of the circuit is reached by constraining the nominal operating range to only 57 % (1.2 V) of the maximum output swing. Within the nominal differential output swing of up to 1.2 V, the deviation of the output voltage from the ideal value (with constant gain A_V = 1.5) is less than 4.5 %. The corresponding nominal differential input swing is 830 mV. Note that the simulated AC-voltage gain factor of 1.4 is a bit smaller than the DC-gain factor of 1.5 because of non-settled thermal transients of the differential path transistors in AC operation.

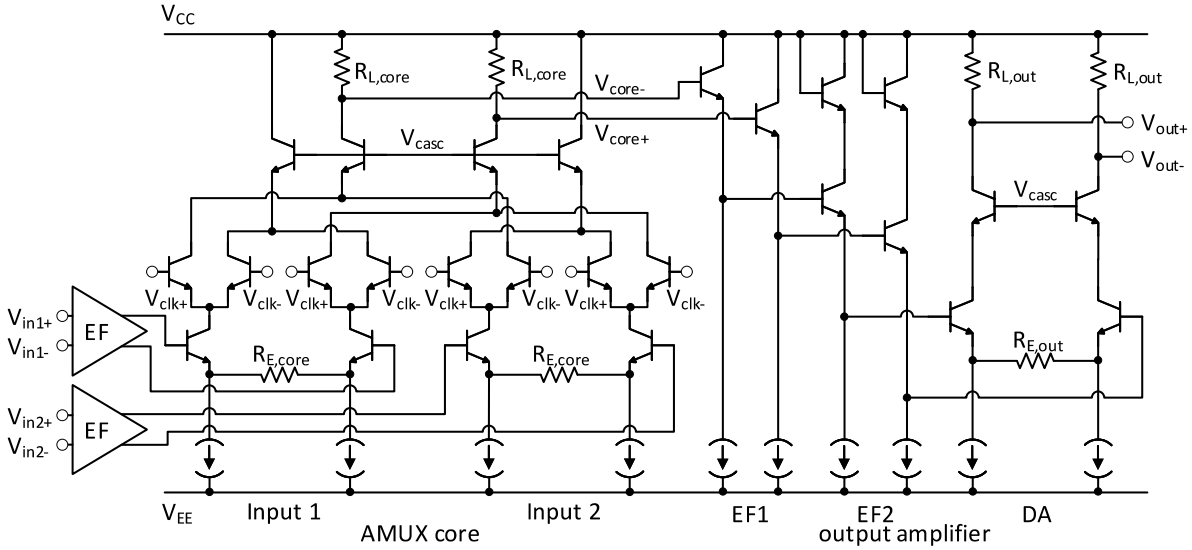

Fig. 3. Schematic of AMUX core and output amplifier.

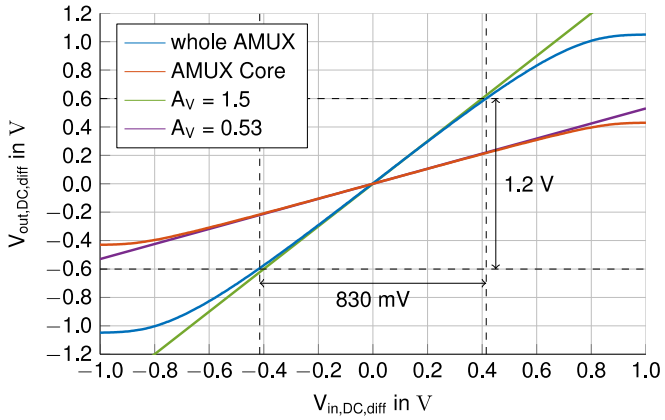

Fig. 4. Simulated static transfer characteristic of the AMUX. Curves for AMUX core without output amplifier and whole AMUX with output amplifier. The linear nominal operating region is indicated by dashed lines.

IV. Measurement Results

The S-parameters measurements are performed directly on the die, with probes and cables deembedded by calibration. Two types of measurements are conducted: Single-ended S-parameters up to 110 GHz and differential S-parameters up to 67 GHz. The nominal supply voltages are −4.5 V for the AMUX core and output amplifier and −3.4 V for the clock buffer. Nominal voltages are used for the single-ended measurement. For the differential measurements, slightly increased voltages of −5.0 V resp. −3.5 V are used. The total power consumption is 1.07 W for nominal voltages and 1.22 W for increased voltages.

Fig. 5 shows the single-ended transmission parameters S_{21} of the transparent signal path. For this measurement, the clock inputs are biased with a DC voltage, so one differential signal input is permanently switched to the output. The unused input and output pins are terminated with 50 Ω. Two configurations for the measured transmission path are distinguished: From inverting input V_{in1-} to inverting output V_{out-} (even) and from noninverting input V_{in1+} to inverting output V_{out-} (odd). For higher frequencies, the circuit behaves differently for both configurations because of the limited common-mode rejection of the two differential amplifiers in the signal path.

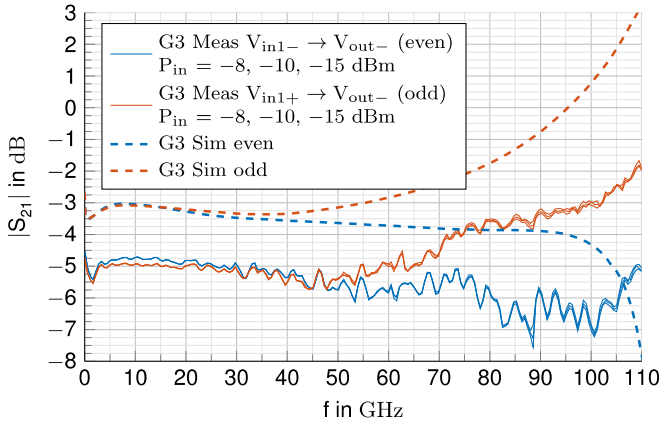

Fig. 5. Single-ended signal path transmission S_{21}. Measurement for different input powers and small signal simulation of SG13G3 chip. Pin configurations “even” and “odd”.

The maximum single-ended input power in this measurement is −8 dBm, which is 4.35 dB below the nominal value of −3.65 dBm ($\widehat{V}_{SE}$ = 415 mV), so only 60 % of the nominal voltage range is used. However, in this range a high linearity can be concluded from the power independence of the S-parameters, which are very similar for the input power levels of -8, -10 and -15 dBm, confirming the linearity simulation results in Fig. 4. S-parameter simulations are conducted after parasitic extraction including EM-simulation of transmission lines. The course of the measured curves agrees quite well with the simulation, but an offset of -2 dB of measurement versus simulation is present.

Fig. 6 shows the differential transmission S_{21} of the transparent signal path. For the single-ended measurements, all four combinations of input 1 and output pins are measured, so the quasi-differential mixed-mode S-parameters of the linear circuit can be calculated up to 110 GHz. The measured transmission is very flat up to 110 GHz. Further, a good agreement between the differential S-parameters up to 67 GHz and the mixed-mode parameters can be observed. Compared to the simulation, there is again about 2 dB less gain, further the simulation exhibits a stronger gain increase for high frequencies. The simulated peaking beyond 110 GHz is mainly attributed to the AMUX core, where the forward coupling through the base-collector capacitance of the differential amplifier provides an additional signal current path for high frequencies. In future designs, the peaking could be emphasized even more, to compensate for the additional frequency roll-off of IC packaging and DACs, as also shown in [8]. The AMUX in the older SG13G2 technology shows 2 dB less gain and an attenuation of 2.2 dB up to 67 GHz. The measured and simulated curves in SG13G2 differ by 2.75 dB but have the same course.

Fig. 7 shows the reflection and isolation parameters of the signal path. The input reflection S_{11} behaves differently for single-ended and differential excitation. This is due to the not perfectly AC-grounded input termination network, thus an additional impedance appears in series to the termination resistor for single-ended measurements. For the intended differential operation, the S_{11} magnitude stays below −15 dB up to 67 GHz. The output reflection S_{22} stays below −9 dB up to 110 GHz. The attenuation/isolation of the inactive signal path is around −35 dB up to 80 GHz.

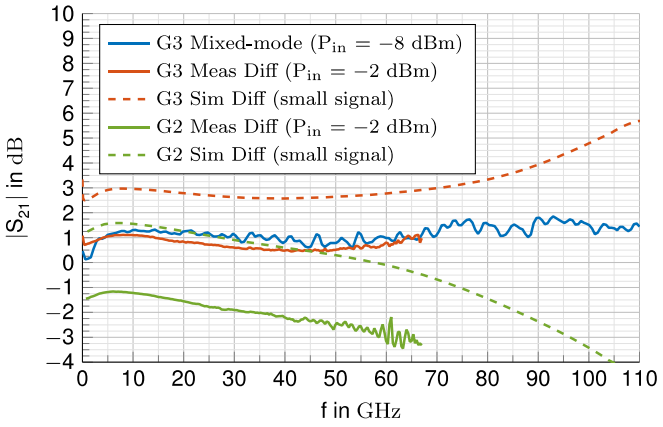

Fig. 6. Differential and calculated mixed-mode signal path transmission S_{21}. Two measurements for SG13G3 chip compared to SG13G2 and small signal simulation. Input power indication is single-ended.

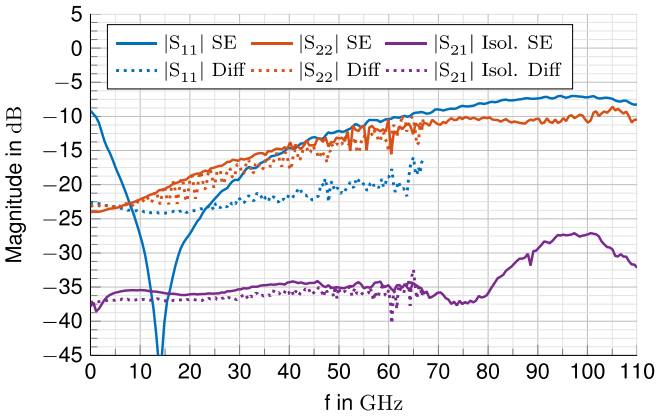

Fig. 7. Measured reflection coefficients S_{11} and S_{22} and transmission S_{21} for the inactive signal path of SG13G3 chip.

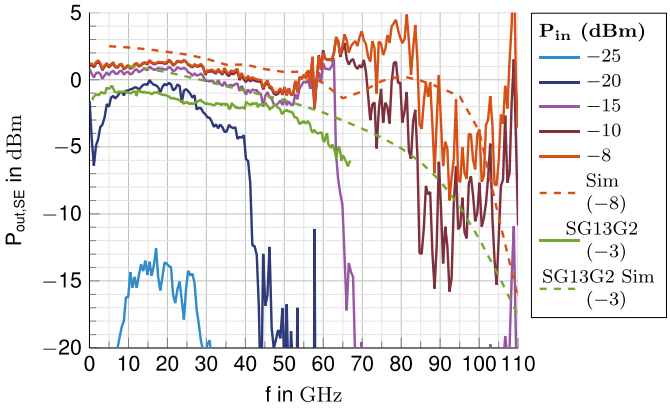

Fig. 8. Single-ended clock path output power for different input powers. Compared to differentially measured SG13G2 chip and large signal simulation. All input and output power indications are single-ended.

For the clock path measurements, static differential voltages of +500 mV and −500 mV are applied to the signal inputs, whereas the network analyzer is connected to the clock input und AMUX output (single-ended). The other clock and output pins are terminated. “Even” and “odd” configuration is not relevant for the clock path, because the asymmetries for single-ended excitation due to limited common-mode rejection average out over the nine differential amplifiers in the clock path. Fig. 8 shows the measured output power versus frequency for different input power levels. For an ideal limiting amplifier, the same output power independent of input power would be expected. However, for very low signal power, asymmetries and noise become predominant and push the amplifier into static limitation. Therefore, for the input powers of −15 dBm and below, a steep descent of output power beyond a certain corner frequency is noticeable, where the clock amplifier does not work properly anymore. As the AMUX will be operated with clock input power well above −8 dBm, no drastic drop is expected. The 3-dB-bandwidth for −8 dBm input power is 85 GHz. The comparison to the circuit in the older SG13G2 technology shows, that the circuit in the new technology increases the bandwidth from 60 GHz to at least 85 GHz with much more clock power especially in the range between 50 GHz and 85 GHz. Note that the measurement for the SG13G2 chip was performed differentially with higher input power level.

V. Conclusion

A 2:1 AMUX implemented using a new SiGe BiCMOS technology generation exhibits remarkable performance gains over the previous technology generation. The circuit has high linearity with output swing up to 1.2 V and 1 dB voltage gain for low frequencies, compared to -1 dB gain with the previous technology. S-parameter measurements show a flat signal path transmission up to at least 110 GHz and clock path 3-dB-bandwidth of at least 85 GHz whereas the AMUX in the previous technology has 2.2 dB attenuation up to 67 GHz in the signal path and 60 GHz clock path bandwidth. With the demonstrated frequency domain performance, the presented circuit offers the potential for time domain signal generation towards 200 GBaud, combining SiGe analog multiplexer circuits with fast DACs using either SiGe BiCMOS or CMOS technology. Time domain measurements including further performance and linearity assessment will be done shortly.

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