This manuscript is published in

IEEE Journal of Solid-State Circuits

Reference:

D. Widmann, T. Tannert, X.-Q. Du, T. Veigel, M. Grözing and M. Berroth, "A Time-Interleaved Digital-to-Analog Converter up to 118 GS/s With Integrated Analog Multiplexer in 28-nm FD-SOI CMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 59, no. 3, pp. 908-922, 2024.

DOI: 10.1109/JSSC.2023.3310381

A Time-Interleaved Digital-to-Analog Converter up to 118 GS/s with Integrated Analog Multiplexer in 28-nm FD-SOI CMOS Technology

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***Abstract*—To enhance sampling rates of CMOS digital-to-analog converters (DACs), analog multiplexing of several DAC output signals in time domain provides a solution. In this paper, a full CMOS integration of two sub-DACs and an active analog multiplexer (AMUX) on a single chip in 28-nm fully-depleted silicon-on-insulator CMOS technology is presented for the first time for sampling rates of 100 GS/s and beyond. Sampling rates up to 108 GS/s for broadband pulse-amplitude modulated signals and up to 118 GS/s for oversampled signals are shown outperforming previously reported data in terms of sampling rate or data rate, respectively. Two 8-bit sub-DACs up to 59 GS/s with CMOS inverter-based output drivers and pseudo-segmentation provide the analog input data for the 2:1 AMUX realized in current-mode topology. An additional on-chip memory of 256 kB completes the system to a universal arbitrary waveform generator. At 100 GS/s, the total power consumption is about 4 W. Generally, an AMUX is able to shift the limits of DACs in well-established CMOS technologies towards higher frequencies independent on technology advances and opens a second, conceptual path for achieving higher sampling rates with an additional benefit of a principle bandwidth extension by the AMUX operation.**

***Index Terms*—Analog-digital integrated circuits, analog multiplexer, arbitrary waveform generator, CMOS integrated circuits, digital-analog conversion, digital-to-analog converter, mixed-signal integrated circuits, pulse-amplitude modulation, transmitters.**

I. Introduction

THE on-going growth of global data traffic drives optical data transmission systems beyond $1\,\mathrm{Tbit/s}$ per wavelength [1]. Digital-to-analog converters (DACs) in transmitter (Tx) front-ends are critical parts for the realization of such systems requiring sampling rates f_s in the range of $100\,\mathrm{GS/s}$ and beyond. For monolithic integration with digital signal processors (DSPs), CMOS DACs are essential. One concept for increasing sampling rates is analog multiplexing of several DAC output signals in time domain using a clocked analog multiplexer (AMUX). The inherent nonlinear operation of an AMUX enables true bandwidth extension on principle due to a real shift of the $\sin(x)/x$ roll-off towards higher frequencies compared to linear active or passive summation of DAC signals. I.e., the -4-dB $\sin(x)/x$ roll-off at the non-return-to-zero (NRZ) sub-DACs' Nyquist frequencies is shifted to the Nyquist frequency of the AMUX. It has already been shown in hybrid systems, e.g. with CMOS DACs and silicon-germanium (SiGe) bipolar AMUXs [2] but no monolithically integrated DAC-AMUX CMOS solution has been reported at comparable conversion rates. In this paper, a full CMOS integration of two 8-bit sub-DACs and an active AMUX on a single chip is presented for the first time for $100\,\mathrm{GS/s}$ and beyond to the best of the authors' knowledge. Multiplexing in analog domain is a flexible solution to further boost the sampling rate and bandwidth of any given CMOS DAC architecture in front of it. In this work, broadband pulse-amplitude modulated (PAM) signals up to Nyquist frequency are demonstrated up to $108\,\mathrm{GS/s}$ (PAM-2) with data rates up to $240\,\mathrm{Gbit/s}$ ($80\,\mathrm{GS/s}$, PAM-8). Moreover, the DAC system can be used for oversampling applications and pulse shaping for sampling rates up to $118\,\mathrm{GS/s}$ at lower symbol rates. Maximum sampling rate as well as data rate outperform previously reported data. Two sub-DACs with CMOS inverter-based output stages being fully compatible to static CMOS logic supply voltage provide analog symbols to an AMUX. The sub-DACs up to $59\,\mathrm{GS/s}$ being implemented in CMOS logic which is modified by resistive feedback in some parts allow compact and dense layout and avoid transistor stacking topologies. A current-mode topology based AMUX with inductive peaking shifts the limits of DACs in well-established CMOS technologies towards higher frequencies independent of technology advances and therefore opens a second, conceptual path for achieving higher sampling rates. Moreover, it is applicable to any sub-DAC architecture. Consequently, it is a conceptual benefit for CMOS Tx circuits. The circuit is realized in 28-nm fully-depleted silicon-on-insulator (FD-SOI) CMOS technology and an additional on-chip 256-kB SRAM memory completes the system to a universal, single-chip arbitrary waveform generator (AWG).

This article is organized as follows. Section II describes the overall system. Circuit implementation details are discussed in Section III. In Section IV, aspects of the applied predistortion are presented. Measurement results are given in Section V separated into static and dynamic characterization according to IEEE standard [3] as well as PAM measurements followed by a comparison to the state of the art and a conclusion.

This project is funded by the *Deutsche Forschungsgemeinschaft* (DFG, German Research Foundation) — 276016065.

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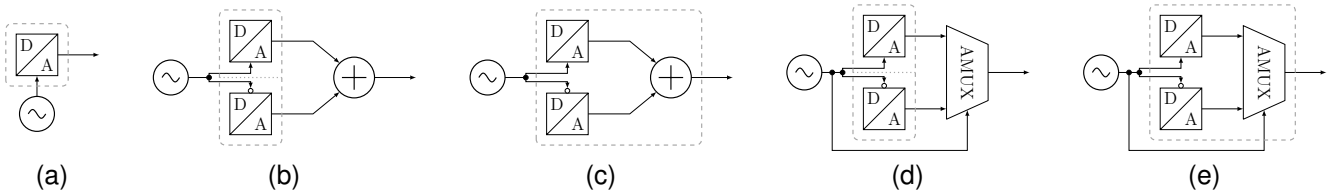


Fig. 1. Concepts for performance enhancement of DACs [1]. Dashed boxes represent system integration, preferably in CMOS technology for (b) to (e). (a) Serial DAC in a faster technology than CMOS (e.g. with SiGe heterojunction bipolar transistors in BiCMOS technology or InP double-heterojunction bipolar transistors). In (b) to (e), realizations of time-interleaved concepts for two DACs are shown for hybrid ((b) and (d)) as well as monolithic ((c) and (e)) systems with non-clocked signal summation ((b) and (c)) and clocked analog multiplexing ((d) and (e)).

II. Concept and System Overview

Fig. 1 summarizes different concepts for performance enhancement of DACs, here exemplarily for two DACs albeit easily extendable to N DACs. Figures 1b to 1e depict interleaving concepts of DACs in time domain at different level of integration. Examples for the realizations according to Fig. 1a can be found in [4] at $100\,\mathrm{GS/s}$, in [5] at $128\,\mathrm{GS/s}$ as well as in [6] at $134\,\mathrm{GS/s}$. In hybrid concepts (Fig. 1b and 1d), different technologies for the DACs and the interleaving circuit may be applied.

Generally, time interleaving might lower the demands on performance of the sub-DACs [7]. A detailed analysis of interleaved DACs is given in [8] where hold-interleaving, data-interleaving as well as data- and hold-interleaving concepts are discussed. It is also referred to as interleaving of return-to-zero (RZ) or NRZ DACs [7], [9] or in general as parallel-path DAC [10]. In these concepts, the sub-DAC signals are summed up at the output which is depicted in Fig. 1b and 1c. Despite the achievement of an increased sampling rate and thus an increased usable bandwidth by linear superposition of phase-shifted sub-DAC signals in these concepts, the analog bandwidth remains constant. It is still limited by the DACs' low-pass characteristics as well as their $\sin(x)/x$ roll-offs. There is still an advantage due to image rejection and oversampling [8], [10] but the symbol rate does not increase accordingly [9]. E.g., the first zero in the frequency response of a 50-GS/s NRZ DAC at $50\,\mathrm{GHz}$ does not change in a 2:1 linear, time-interleaved system of two DACs with a total sampling rate of $100\,\mathrm{GS/s}$. It is determined by the sub-DACs. On the other hand, time interleaving of RZ sub-DACs does not suffer from this limitation. However, the requirements to these sub-DACs are enhanced compared to NRZ sub-DACs. On the contrary, time interleaving by an AMUX provides a $\sin(x)/x$ roll-off shift according to the interleaving factor independent on the $\sin(x)/x$ roll-off of the individual NRZ sub-DACs. Therefore, it is capable of providing a true bandwidth extension towards higher frequencies. By changing the circuit topology compared to the sub-DACs, even other limiting low-pass characteristics can be improved. An implementation of a parallel-path DAC at $250\,\mathrm{MS/s}$ is shown in [10]. In [11], the concept of Fig. 1b is presented at $200\,\mathrm{GS/s}$. Moreover, a realization of Fig. 1c is reported in [12] at $100\,\mathrm{GS/s}$. Hybrid time interleaving by an AMUX according to Fig. 1d is shown in [13] at $56\,\mathrm{GS/s}$, in [14] at $100\,\mathrm{GS/s}$, in [15] at $120\,\mathrm{GS/s}$, in [16] at $120\,\mathrm{GS/s}$ and $150\,\mathrm{GS/s}$, in [17] at $160\,\mathrm{GS/s}$ as well as in [18], [19] at $168\,\mathrm{GS/s}$. Moreover, a 4:1 concept at $100\,\mathrm{GS/s}$ is presented in [20], [21]. Finally, a CMOS DAC based setup corresponding to Fig. 1d consisting of two CMOS DACs at $90\,\mathrm{GS/s}$ each and a SiGe heterojunction bipolar transistor AMUX is reported in [2] with a total symbol rate up to $120\,\mathrm{GBaud}$. The concept of an integrated AMUX has already been implemented in [7] at $11\,\mathrm{GS/s}$ in 28-nm CMOS or in [22] at $28\,\mathrm{GS/s}$ in 16-nm CMOS.

In this work, concept 1e is pursued. Fig. 2 shows a block diagram of the entire system. Two SRAM memories with $128\,\mathrm{kB}$ each provide the data for the two sub-DACs with nominal resolutions of $8\,\mathrm{bit}$ and sampling rates up to $59\,\mathrm{GS/s}$. Their analog outputs are time-interleaved by the AMUX yielding sampling rates of up to $118\,\mathrm{GS/s}$. Digital data of the memory is transmitted in parallel via 256 differential lines at a rate of $f_\mathrm{s}/32$ to the sub-DACs. Fig. 3 shows the operation principle in more details and a timing diagram. To ensure maximum margin for timing inaccuracies, the DAC output signals are sampled by the AMUX in the center of each hold period [9]. With the AMUX being opaque during sub-DAC switching, glitches, jitter or other sub-DAC artifacts are suppressed in the output signal to a certain degree assuming the AMUX itself does not contribute other significant artifacts. The sub-DACs as well as the AMUX operate at half-rate clock. An input offset control circuit (clk offs) adjusts the duty cycle of the differential input clock signal for the AMUX adapting the symbol durations of positive and negative clock half-waves. Timing adjustment between sub-DACs and AMUX is controlled by two 5-bit programmable phase rotators (ϕ_0, ϕ_1) in $f_\mathrm{s}/4$ domain operating in all four quadrants. For conceptual reasons, 28 different phases are applicable, i.e. at $118\,\mathrm{GS/s}$, ideally $\sim 1.2\,\mathrm{ps}$ timing steps can be set if equally spaced phase positions are assumed. Prior to the sub-DAC clock inputs, a level conversion circuit from current-mode to CMOS topology voltage levels including common-mode control (CM_0, CM_1) is implemented. The main emphasis of this work is on reaching highest sampling and data rates rather than any power consumption considerations.

III. Circuit Implementation

The sub-DACs as well as the AMUX are implemented as differential circuits based on transistors with flipped wells [23], [24]. In all high-frequency circuit parts, i.e. the clock path, the sub-DACs and the AMUX, forward body-biasing

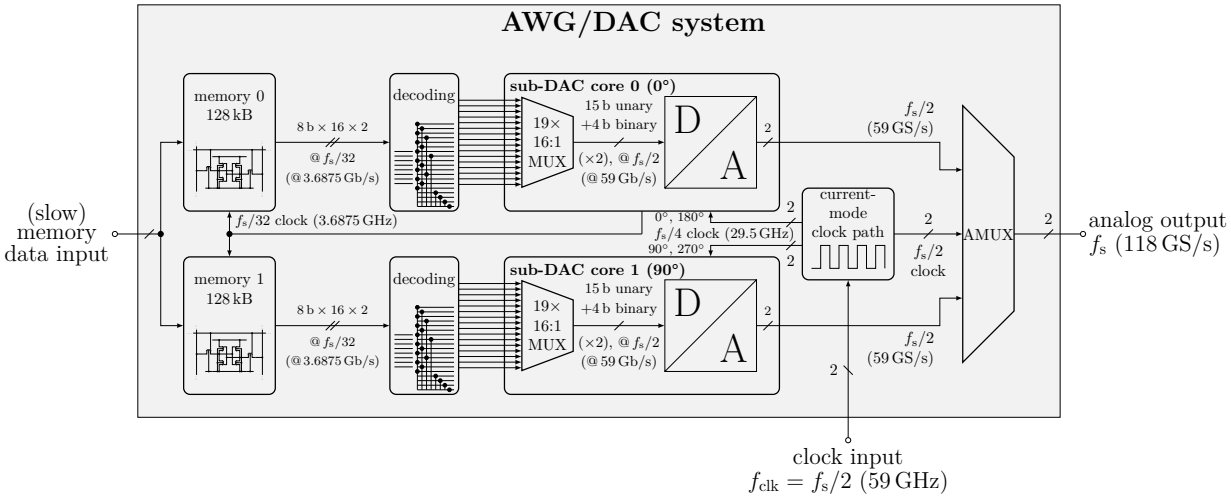
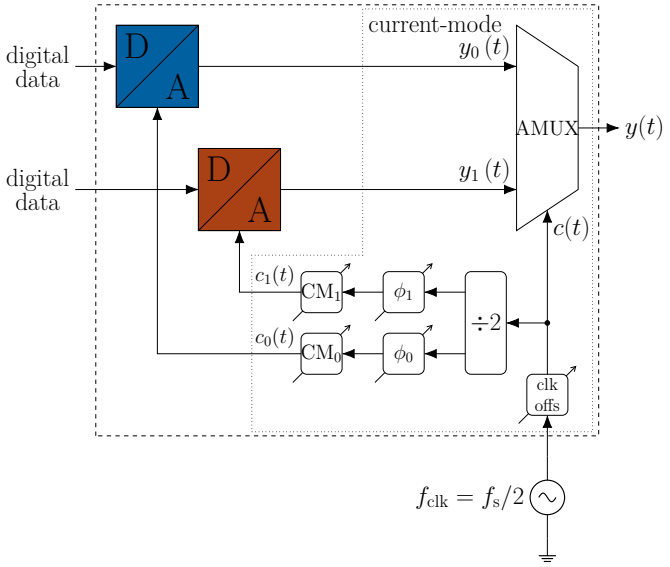


Fig. 2. AWG/DAC system overview. Two memory blocks with 128 kB each provide the data for the two sub-DAC cores with a nominal resolution of 8 bit. The analog outputs of the sub-DACs are combined by an active AMUX. Values in brackets are given for 118-GS/s operation.

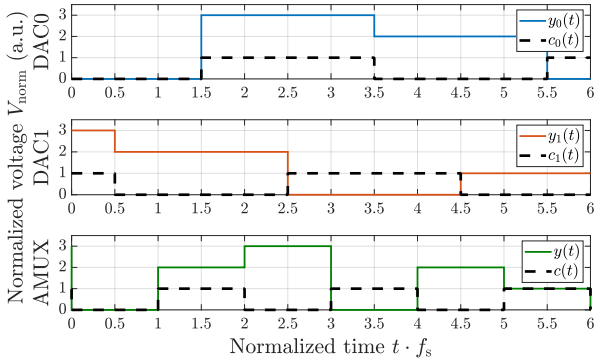
(FBB) is used to lower the transistors' threshold voltages and to boost high-frequency performance. Global FBB in the sub-DACs is provided by an external supply from ± 1.8 V ($\leq$100 GS/s) up to ± 3.0 V (>100 GS/s). FBB in the current-mode parts is generated on-chip from the respective supply voltage according to transistor stacking. In the memory, no FBB is applied. Concerning topology, the system can be divided into two parts. The DAC cores, the memory as well as the clock path at lower frequencies (part of $f_s/4$ clock path and lower) are implemented in modified CMOS logic family concepts extended by resistive feedback methods. Parts operating at $f_{clk} = f_s/2$, i.e. the respective clock path as well as the AMUX, are realized in (inductively peaked) current-mode topology using shunt peaking or a combination of shunt and series peaking [25], [26]. Additionally, the frequency divider to $f_s/4$, the phase rotators (ϕ_0, ϕ_1) and the current-mode-to-CMOS interface circuits (CM_0, CM_1) between the two circuit topologies belong to the current-mode part. A detailed description of the broadband current-mode clock path is given in [27] with improved functionality from DC up to 60 GHz in case of the work presented here.

A. Digital-to-Analog Converters

The sub-DAC cores are implemented (pseudo-)differentially. In the sub-DACs with a nominal resolution of 8 bit, a pseudo-segmented approach is applied [28], [29]. The four least significant bits (LSBs) are realized in an R-$2R$ part with inherent binary weighting. The four most significant bits are represented by 15 unary paths like a thermometer DAC. However, a passive binary-weighting decoder instead of a thermometer decoder is used implemented as wiring block in the $f_s/32$ domain. I.e., a decoding stage connects the unary paths according to Fig. 4 resulting in a binary weighting. In total, 19 data paths represent the digital 8-bit word of each sub-DAC. The passive decoding network is implemented in front of the sub-DACs as depicted in Fig. 2. The unary part is connected in an alternating manner to reduce gradient effects [28], [29]. Fig. 5 illustrates the block diagram of one sub-DAC core. The clock path consists of three frequency dividers as well as driver cascades. The first frequency divider for $f_s/4 \rightarrow f_s/8$ immediately starts with the applied clock signal from the current-mode clock path and an adapted clock path initialization and starting circuit ensures proper starting conditions. The frequency dividers for $f_s/8 \rightarrow f_s/16$ and $f_s/16 \rightarrow f_s/32$ include logic for synchronous start and reset (R_0/R_1) which ensures a defined phase relation of the two sub-DACs in combination with a proper starting concept. I.e., the frequency dividers from $f_s/4 \rightarrow f_s/8$ start synchronously on principle due to defined initialization. In addition, the common reset signals of both sub-DACs R_0/R_1 are sampled ensuring synchronous start of the lower frequency domains. Precise clock phase alignment of the different clock frequency domains is adjusted by CMOS inverter chains. Delay adjustment is done at the beginning of the CMOS inverter chains using transistor widths of 4 µm and 8 µm for nFET and pFET, respectively, for power consumption reasons. At the end of the inverter chains, the fan-out is increased ending up in the required driver capability with transistor widths of 80 µm and 160 µm for nFET and pFET, respectively. The length as well as the size of the driver chains especially in $f_s/4$ domain is a major challenge. Duty cycle and common-mode stability are enhanced by resistive feedback. Supply voltage is stabilized by on-chip decoupling capacitance. The clock lines driven by large output drivers of the clock network form artificial transmission lines in combination with the capacitive load given by the local clock drivers at each tap. Due to long inverter chains in the clock network, resistive feedback across three inverters is used as shown in Fig. 6. Resistive feedback across one inverter is a well-known concept known from transimpedance amplifiers using feedback inverter cells [30]–[32] and is also applied in DAC implementations (e.g. [33]). Here, it is applied to increase performance, i.e. bandwidth and common-mode stability. Considering an inverter chain as amplifier, a proper trade-off between gain and bandwidth is sought. Resistive



(a)



(b)

Fig. 3. (a) Block diagram of the time-interleaved system with two sub-DACs and an AMUX as well as (b) ideal operation in time domain for non-delayed zero-order hold signals with half-rate clocks. In (a), a clock offset affecting the AMUX symbol durations of positive and negative half-waves, the sub-DAC phases ϕ_0 and ϕ_1 as well as the common-mode levels CM_0 and CM_1 can be adjusted.

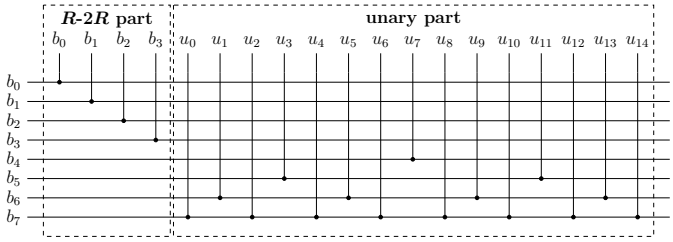


Fig. 4. Passive decoding network for the pseudo-segmented architecture [28], [29]. It shows the mapping of the 8 bits $b_0, \ldots, b_7$ to the 19 DAC channels: R-$2R$ part $b_0, \ldots, b_3$ and unary part $u_0, \ldots, u_{14}$.

feedback across three inverters is based on a different trade-off compared to a three-stage cascade of three inverters with individual feedback. It provides bandwidth extension compared to a chain without feedback but less bandwidth than a chain of inverters with individual feedback. The latter is also dependent on the resistor value. It is still negative resistive feedback. However, compared to resistive feedback across each inverter,

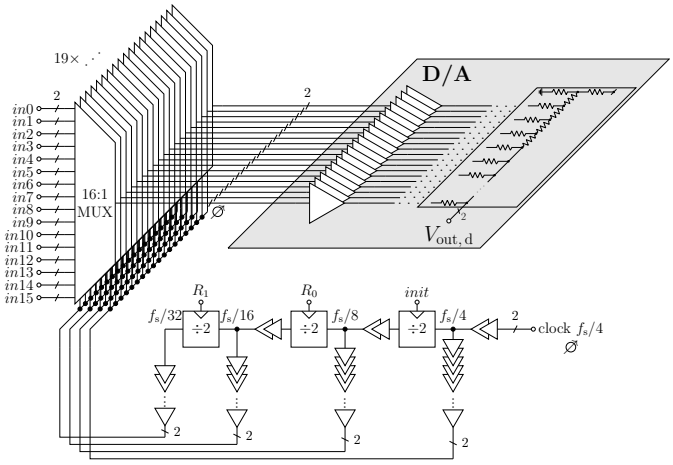


Fig. 5. Block diagram of one sub-DAC core. Common-mode voltages can be measured at the positions marked by $\varnothing$.

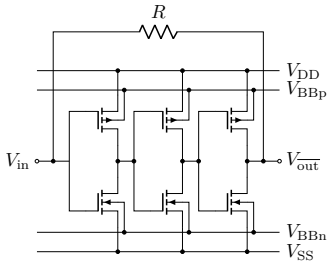


Fig. 6. Resistive feedback concept in the clock driver chains of the sub-DACs. V_BBn and V_BBp represent the body-biasing voltages for forward body-biasing.

the power consumption is lower as the first and the second inverter do not drive a static load (leakage neglected). Moreover, a single resistor for three inverters reduces area consumption and the gain is higher as the voltage levels are recovered by the first and the second inverter. The value of the feedback resistor R is chosen as $R \approx 3\,\mathrm{k\Omega} \cdot \mu\mathrm{m}/W_\mathrm{n}$, where W_n denotes the smallest nFET width in the chain. The value provides enhanced inverter chain performance across corners and is large enough to prevent the circuit from oscillating. The driving stage before is always capable of forcing the stage into a static, defined state. In summary, this feedback concept provides a good trade-off between bandwidth enhancement, common-mode stability, output swing and (static) power consumption.

In the data path, digital 16:1 multiplexers (MUX) realized in a tree structure provide data at $f_\mathrm{s}/2$ to the output stage as shown in Fig. 7a. The tree structure is repeated for all 19 data channels in each sub-DAC. All MUX stages consist of a five-latch MUX (Fig. 7b) [34] operating at half-rate clock with a timing diagram depicted in Fig. 7c. The design ensures that the sum of the clock-to-output time of the latches and the delay through the transmission gate transistors realizing the MUX operation, i.e. the total data signal's latency, is in compliance with the setup time of the following flip-flop. For each branch, the clock frequency is divided by two compared to the subsequent stage. To keep the load of the global clock

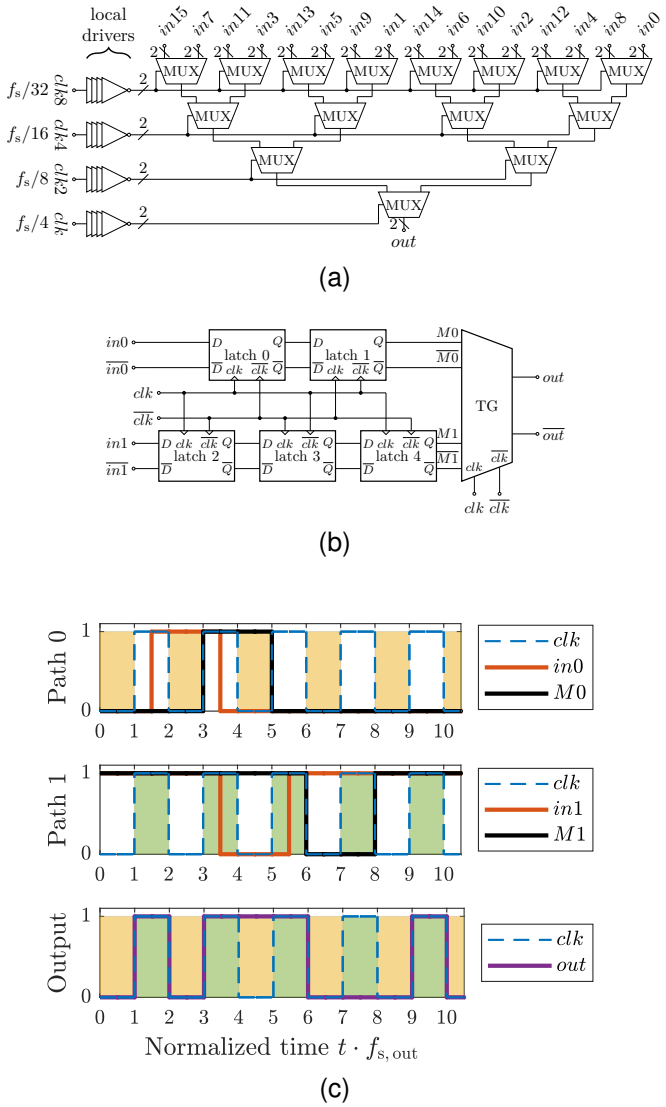


Fig. 7. (a) MUX tree resulting in a 16:1 serializer and (b) single MUX stage [34] with (c) corresponding timing diagram. Input inverters at each MUX stage are not drawn. For clk = H, latches are in opaque mode and for clk = L, they are transparent. Local drivers at each MUX tree reduce the load of the global clock network. The frequency $f_{s,\,out}$ corresponds to the output data rate at the output of each MUX stage.

network constant, the transistor widths in the MUX stages are scaled down by a factor of two while the number of MUX stages is doubled with each new branch. All MUX stages consist of five latches and transmission gates (TG) executing the MUX operation. The latches ensure proper timing at the TGs and reduce glitches at the output.

Following the data path, digital data passes a driver stage using a different resistive feedback concept as shown in Fig. 8a. For bandwidth enhancement and DC operation point stability, a cascade of CMOS inverters with resistive feedback as pre-driver and a last output driver without feedback is used to drive the DAC output network. Resistive feedback reduces data-dependent jitter due to bandwidth increase. As output stage, a CMOS inverter-based structure is used as presented in Fig. 8b. The latter shows the pseudo-segmented structure (4 bit R-$2R$, 4 bit unary) with a total output resistance of 50 Ω (100 Ω differential) for $R = 400\,\Omega$. Unary cells are connected appropriately in the decoder network in front of the serializers. The inverters' output resistances R_o are considered in the $2R$ series resistors of the resistor network. The CMOS inverter-based output structure in combination with the resistor network can be viewed as a voltage-mode DAC providing a nominal single-ended output swing of ∼500 mV at 50-Ω termination or 1 V differentially, respectively. The combination of the last output driver in Fig. 8a and the series resistor $2R - R_o$ in Fig. 8b can be regarded as a source unit which is identical for all 19 data channels. It corresponds to source-series terminated (SST) transmitters [35]. Different aspects have to be considered in the design of this output inverter. Firstly, both transistors, NMOS and PMOS, have to behave symmetrically, especially in terms of their output resistance R_o. Secondly, to reduce linearity errors, the transistors have to operate deeply in the linear region to keep the output level dependency of R_o as low as possible which requires low drain-source voltage drops and therefore large channel widths. However, with increasing channel widths, more pre-drivers are required in the output driver stage according to Fig. 8a which increases timing deviations due to increasing distance to the last sampling operation. For this reason, a trade-off is required and a value of $2R - R_o = 700\,\Omega$ is chosen, i.e. $R_o = 100\,\Omega$. This specification corresponds to an nFET width of $W_{no} \approx 4\,\mu m$ and a pFET width of $W_{po} \approx 9\,\mu m$ for the output drivers. The driver cascade in Fig. 8a adapts the driver capability starting from 1 µm and 2 µm of nFET and pFET width of the first CMOS inverter, respectively. Feedback resistors are chosen according to $\sim 5\,k\Omega \cdot \mu m / W_n$ where W_n denotes the nFET width of the corresponding inverter. To keep the load of the driving stage inverters constant, an additional resistor couples the driving stages in front of the output inverters. The output structure of Fig. 8b resembles the voltage-mode driver discussed in [36] where the transistors are operated as low-impedance switches, i.e. a low impedance compared to the linear resistors. It is also referred to as SST driver in [33], [35], [37]–[40] with a common series resistor at the output of the CMOS inverter or series resistors between the drains of the transistors. Finally, a major advantage of the CMOS inverter-based topology omitting transistor stacking is a full compatibility of the sub-DACs to CMOS logic circuits such as DSPs in terms of supply voltage.

B. Analog Multiplexer

The schematic of the active AMUX is presented in Fig. 9 and is based on a source-coupled circuit topology similar to [13]. Transistor widths for data and clock inputs are 90 µm and 60 µm, respectively. Degeneration resistors have a value of $R_s \approx 6.5\,\Omega$ and the tail current sources provide $I_0 \approx 30\,mA$. Basically, it consists of two interleaved Gilbert cells. At the bottom, two linearized transconductance stages serve as data inputs. Above, cascode current switches driven by the differential half-rate clock signal are stacked performing the nonlinear operation and directing the respective data input stage either to the output path or to a dummy path by current steering.

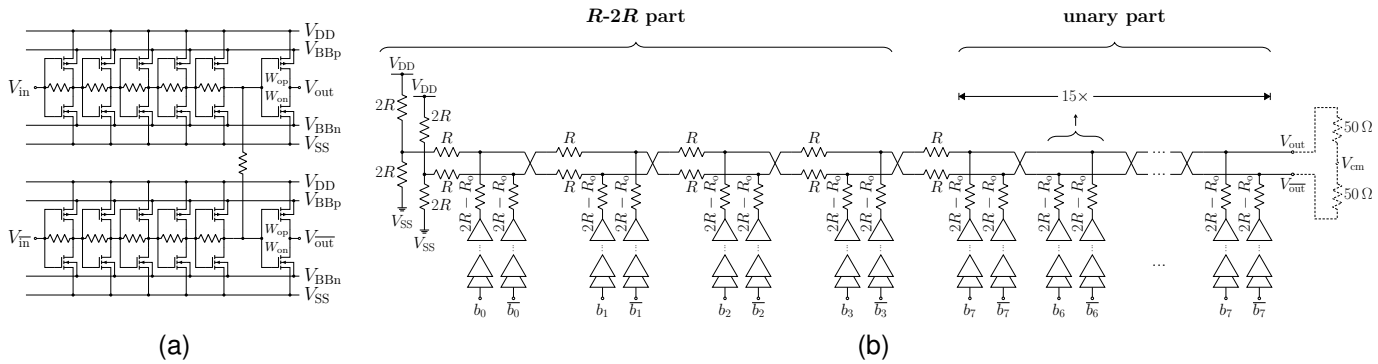


Fig. 8. (a) Output driver stage in the sub-DACs and (b) schematic of the output network realizing the digital-to-analog conversion with driver stages according to (a) and a resistor network. Unary paths are connected in an alternating arrangement b_7-b_6-b_7-b_5-b_7-b_6-b_7-b_4-b_7-b_6-b_7-b_5-b_7-b_6-b_7.

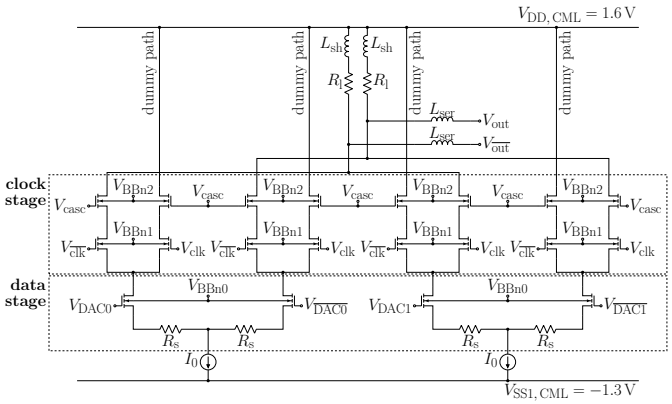
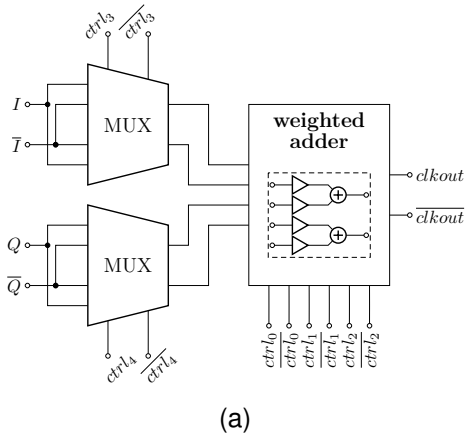


Fig. 9. Schematic of the AMUX.



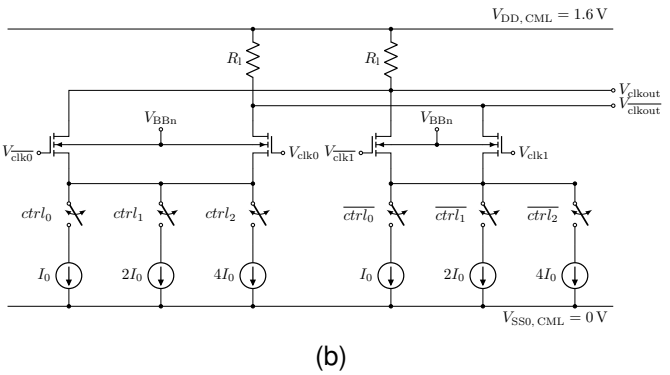


Fig. 10. Implementation of the quadrature phase rotators. (a) MUX stage selecting the quadrant and (b) phase interpolator.

The load resistors have a value of $R_\mathrm{l} = 50\,\Omega$. Shunt and series peaking inductances with $L_\mathrm{sh} \approx 65\,\mathrm{pH}$ and $L_\mathrm{ser} \approx 40\,\mathrm{pH}$ are used to improve the output bandwidth. The inductors are modeled using a 3D planar electromagnetic simulator to get broadband S-parameter models used for circuit simulation. A pad capacitance of $C_\mathrm{pad} \approx 33\,\mathrm{fF}$ is determined for the clock input as well as the analog output signal pads. Additionally, for further enhancement, the output is biased externally to $V_\mathrm{DD,\,CML}$ by bias tees providing the DC current to be able to reduce the load resistors' width to a minimum at lower current budget. This way, the load resistors R_l are only affected by dynamic currents and their widths can be significantly reduced yielding a much smaller parasitic capacitance.

C. Clock Path

Precise timing of the sub-DACs' outputs in relation to the AMUX clock is of particular importance for operation. Two 5-bit programmable phase rotators [27], [41]–[44] (see Fig. 3a) allow clock signal phase tuning at the required resolution. Fig. 10 shows the implementation of the phase rotators operating in all four quadrants. The first frequency divider from $f_\mathrm{s}/2$ to $f_\mathrm{s}/4$ provides four clock phases: I, $\overline{I}$, Q and $\overline{Q}$. In a first MUX stage, two signals with a phase difference of $\pm 90°$ are selected defining the quadrant as a coarse position. In the phase interpolator according to Fig. 10b, the fine interpolation is performed by programmable current sources with binary weighting. Phase interpolation is realized by a weighted summation of the input clock signals. For conceptual reasons, four phases at the corners of the quadrants coincide which is why 28 different phases are available. For proper operation, a phase difference of 180° in $f_\mathrm{s}/2$ clock domain or 90° in $f_\mathrm{s}/4$ clock domain between the sub-DACs is required. To avoid glitches, the signals $ctrl_0, \ldots, ctrl_4$ have to be synchronous.

The implementation of the first CMOS frequency divider from $f_\mathrm{s}/4$ to $f_\mathrm{s}/8$ depicted in Fig. 5 is shown in Fig. 11a. This frequency divider is the most critical part in the clock path being

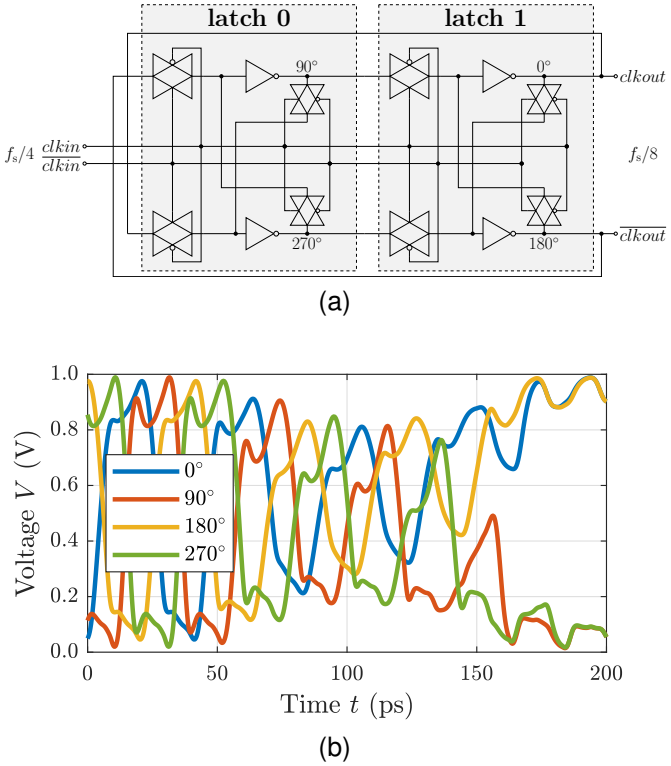


Fig. 11. (a) Implementation of the first CMOS frequency divider. Initialization transistors are not shown. (b) Simulated behavior on schematic level at an input frequency of 48 GHz in case of a critical distortion (here: supply voltage drop).

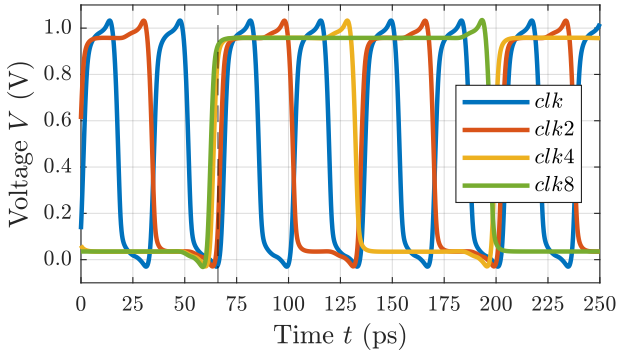


Fig. 12. Simulation of clock signals on schematic level at the output of the clock network in Fig. 5 (single-ended) at $f_s = 118\,\mathrm{GS/s}$. Clock signals correspond to the MUX tree clock inputs in Fig. 7a.

sensitive to supply voltage drops, input clock signal magnitude and common-mode voltage as well as glitches at the start of operation and during a change of the respective phase rotator. Supply voltage stability is addressed by a careful analysis of the required on-chip decoupling capacitance. The input common-mode can be controlled by CM0/CM1 in Fig. 3a. Finally, critical glitches in the clock signals at the start of operation are omitted by a starting circuit which is implemented as a MUX in the current-mode clock path at $f_s/2$ switching from a defined initial static state to the input clock signal by sampling the MUX's switching signal with the input clock. The frequency divider itself is initialized by pull-down transistors (*init* signal in Fig. 5). The transistors at the driver inverter inputs initialize the frequency divider in a defined, valid state, i.e. low at the 0° and 90° nodes while the transmission gates at the input of latch 1 are opaque. Fig. 11b shows the reaction of the divider to one of the mentioned critical distortions. The frequency divider transfers into an invalid state and stops operation permanently. It can only be reactivated by new initialization into a valid state.

The clock signal outputs of the clock network controlling the MUX tree are depicted in Fig. 12. The additional delays added to the higher frequency clock signals shown in Fig. 5 ensure that no flip-flop setup times in the MUX tree of Fig. 7a are violated. Clock signal common-mode voltages at the current-mode-to-CMOS topology interface (CM0/CM1 in Fig. 3a) are controlled by external bias voltages considering that the common-mode levels of the clock signals that can be measured at the nodes ∅ in Fig. 5 correspond to a respective duty cycle. Timing optimization between the sub-DACs and the AMUX is performed by outputting single unit impulses and manually adjusting the 5-bit phase rotators (ϕ_0/ϕ_1 in Fig. 3a) properly with a 90° phase offset with respect to the sub-DACs' clock frequency. Maximum pulse heights and minimum pulse widths of the output pulses determine the best timing conditions.

D. Voltage Domains and Decoupling Capacitances

The conceptually induced highly dynamic load of the static CMOS logic in the sub-DACs requires careful consideration of supply voltage domains and decoupling. Therefore, clock and data voltage domains are separated. Also, the clock network is subdivided into two voltage domains. I.e., clock drivers and frequency dividers are separated as the first CMOS frequency divider from $f_s/4$ to $f_s/8$ is the most critical part in the clock path. Moreover, the data path is subdivided into two domains: the MUXs and the output drivers. As the 19 MUXs cause huge dynamic supply voltage loads, the output drivers are separated to increase analog signal quality. A division of current-mode parts is not required due to constant load by the tail current sources. Furthermore, a cascaded concept for supply voltage decoupling is applied individually for all supply voltage domains. On-chip MOS capacitors stabilize supply voltages and provide high-frequency decoupling with a trade-off concerning area consumption. Moreover, bonding capacitors on the RF board provide further capacitance in close proximity to the chip. Finally, surface-mounted device capacitors are placed on the RF board at larger distance. To further relax load steps in the current consumption on start-up as well as on shutdown, the sub-DACs' clock paths are switched on and off sequentially by the resettable frequency dividers in Fig. 5. On the one hand, it prevents critical supply voltage dips that might lead to a nonfunctional static state of the first CMOS frequency divider. On the other hand, it reduces dangerous voltage peaks on shutdown due to a sudden load reduction in combination with the inherent supply line and bond wire inductances.

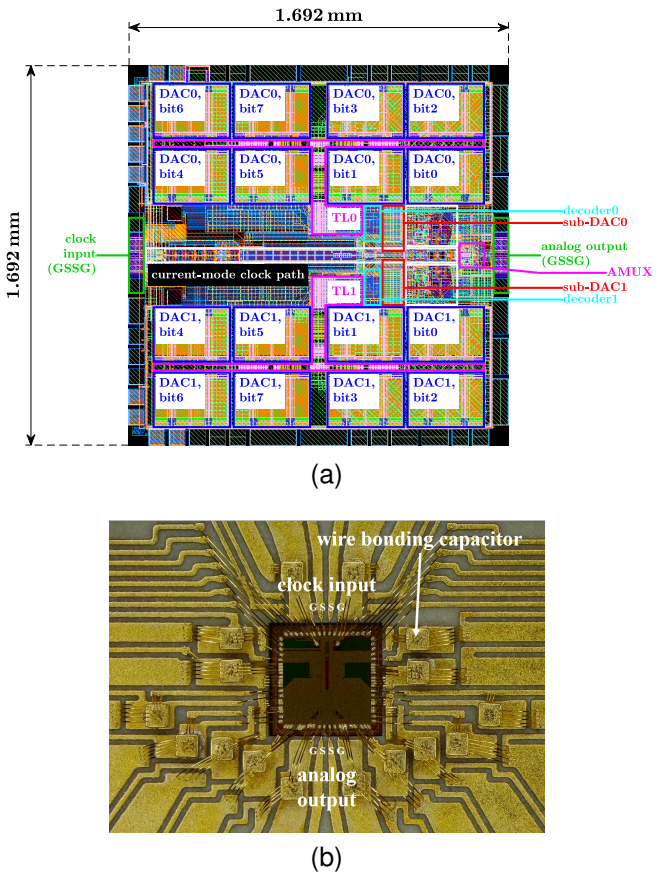


Fig. 13. (a) Layout of the chip with different circuit parts being highlighted and (b) micrograph of the bonded die in RF PCB cavity. Transmission lines TL0/1 denote the data paths from the memory to the sub-DAC cores.

E. Layout and Chip Assembly

Layout and chip assembly are shown in Fig. 13. The die is connected by bond wires. The bond wire diameter is $25\,\mu\text{m}$ with a linear distance of about $250\,\mu\text{m}$ for the output signal bond wires without considering the loop. To reduce the bond wire length, the die is placed inside a cavity in the RF printed circuit board (PCB). Due to high power dissipation, the die is placed on a copper plate using a thermally conductive adhesive. Moreover, thinned dies of about $120\,\mu\text{m}$ thickness are used for thermal reasons. However, experimental results with standard dies of about $250\,\mu\text{m}$ thickness reveal that die thickness is not critical. The substrate material of the board is Rogers RO3003 with a thickness of $130\,\mu\text{m}$. The die size is $\sim 1.9\,\text{mm} \times 1.9\,\text{mm}$ and the areas of one sub-DAC core and the AMUX cover $\sim 215\,\mu\text{m} \times 100\,\mu\text{m}$ and $\sim 127\,\mu\text{m} \times 135\,\mu\text{m}$, respectively. A ground-signal-signal-ground structure is used for the clock input as well as the analog output. No electrostatic discharge protection is implemented at the high-bandwidth inputs and outputs.

IV. Linear, Periodically Time-Varying Predistortion

The measurements in the next section reveal deterministic, linear, periodically time-varying (LPTV) behavior [45]–[48].

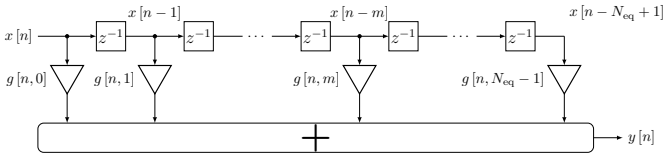


Fig. 14. Discrete-time, time-varying finite impulse response filter applied for LPTV predistortion with an input signal $x\,[n]$ and output signal $y\,[n]$ [49].

These variations correlate to the clock frequencies inside the sub-DACs. Periodic voltage variations have influence on the output sampling in the sub-DACs and affect the analog output symbols deterministically. Hence, an appropriate LPTV predistortion is applied. Given a linear system with system operator $\mathcal{T}$, the continuous-time impulse response $h(t,\tau)$ is defined as the response at observation instant t to an input Dirac impulse $\delta(t-\tau)$ at instant of time τ [49]:

$$h(t,\tau) := \mathcal{T}\{\delta(t-\tau)\}\ . \tag{1}$$

Generally, a two-dimensional function of the two independent variables t and τ has to be considered. The modified, time-variant impulse response or (input) delay-spread function [49], [50] $g\,(t,\gamma)$ is obtained by the transformation of variables

$$\tau = t - \gamma \tag{2}$$

which results in

$$g\,(t,\gamma) := h\,(t, t-\gamma)\ . \tag{3}$$

For an LPTV system with normalized period $P \in \mathbb{N}$, it holds

$$h\,(t + P\cdot T_\text{s}, \tau + P\cdot T_\text{s}) = h\,(t,\tau) \tag{4}$$

and

$$g\,(t + P\cdot T_\text{s}, \gamma) = g\,(t,\gamma) \tag{5}$$

where $T_\text{s} = 1/f_\text{s}$ denotes the sampling period. $P = 1$ represents a linear, time-invariant (LTI) system. LPTV predistortion is applied with the help of the discrete-time modified impulse response $g\,[n,\nu]$ using a classical transversal filter structure as its known from LTI systems with finite impulse response filters. Fig. 14 shows the filter structure for a filter length N_eq. Filter coefficients change periodically in time. The only difference compared to an LTI system is using a two-dimensional lookup table (LUT) of size $P \times N_\text{eq}$ for the filter coefficients accessed via $g\,[(n \bmod P)\,,\nu]$ instead of constant filter coefficients in a vector of size $1 \times N_\text{eq}$. Multiplication and summation operations are the same as for LTI feed-forward equalization (FFE) and can be implemented using conventional arithmetic circuits. Hence, it is compatible to DSPs. In the LPTV case, the multiplication factors change cyclically with period P. Hence, the required DSP memory to store the filter coefficients increases from N_eq numbers in case of an LTI filter to $N_\text{eq}\cdot P$ numbers in case of the LPTV filter. Finally, LPTV predistortion requires the knowledge of the symbol position within one period P. This method is generally applicable to interleaved systems for compensation of channel variations.

Data is generated in offline pre-processing and loaded into the AWG memory. The significant part of mean predistortion

coefficients (LTI case) normalized to the maximum value for the case of $f_s = 100\,\mathrm{GS/s}$ is approximately given as: -0.01, 0.07, -0.30, 1.00, -0.19, -0.06, -0.01, 0.01, 0.00, 0.00, -0.01, 0.01, 0.00, 0.01, 0.00, 0.00, 0.00, -0.01, 0.01, -0.04, 0.06, -0.04. These coefficients slightly vary with a period of $P = 32$ being considered in the LPTV predistortion. The time-variant impulse response is estimated by measuring the impulse reactions at the output to stimulating impulses of one sampling period T_s duration at different memory positions within one period P. From these results, predistortion coefficients depending on the symbol's position can be determined. The mean coefficients shown above reveal that a filter length of about $N_{eq} = 5$ would be sufficient for predistortion of the main impulse. However, due to small reflections caused by assembly around $170\,\mathrm{ps}$ after excitation as it can be observed from the predistortion coefficients, a larger filter length is used in offline pre-processing to achieve best results. After the main impulse, the reflection predistortion becomes obvious in the coefficients separated from the one of the main impulse by a gap of coefficients with essentially zero values. More precisely, a generous filter length of $N_{eq} = 32$ coefficients is used as the filter length is not a critical factor in offline pre-processing but the number of significant predistortion coefficients is well below. Similarly, the chosen period of $P = 32$ could potentially be reduced.

V. Measurement Results

A. Measurement Setup

For measurements, a subsampling oscilloscope with a sampling module input bandwidth of $70\,\mathrm{GHz}$ in combination with a phase reference module driven by the $f_s/2$ clock for low jitter measurements ($<100\,\mathrm{fs}$ RMS) is used. A clock signal generated by an Anritsu MG3697C signal generator is split into two parts by a power splitter. One part is used to drive the phase reference module. The other part is used to drive the circuit and is sent through a broadband balun (Hyperlabs HL9407) and DC blocks in the 1.85-mm system to the RF PCB via Mini-SMP connectors. RF lines on the RF PCB guide the differential clock signal via bond wires to the chip. The differential analog output signal travels through the output bond wires, the RF PCB, Mini-SMP connectors, cables and broadband bias tees (SHF BT65R) to the Tektronix DSA8300 with 80E11 sampling modules. Fig. 15 shows the measurement setup. For the analysis of single-tone signals, the oscilloscope is run in a combined mode using the phase reference as well as the prescale trigger to get traces in equivalent time. Current-mode parts operate at $1.6\,\mathrm{V}/-1.3\,\mathrm{V}/-0.6\,\mathrm{V}$ and CMOS parts at $1.0\,\mathrm{V}$ nominal ($1.15\,\mathrm{V}$ overdrive). Close to the chip, the supply voltages are nominal or slightly subnominal except the voltage of the digital MUXs. For this domain, a voltage of roughly $1.1\,\mathrm{V}$ is applied at highest sampling rates $\geq 100\,\mathrm{GS/s}$.

B. Static Characterization

Static characterization is done for both sub-DACs individually. The output signals still travel through the AMUX but the AMUX clock signal is set to a static state which is why the AMUX acts as a linearized amplifier while the sub-DAC clocks are runnning. From the measured transfer function, differential nonlinearity (DNL) as well as integral nonlinearity (INL) are extracted and the reults are given in Fig. 16. The INL is referred either to the end-point line or to a best-fit

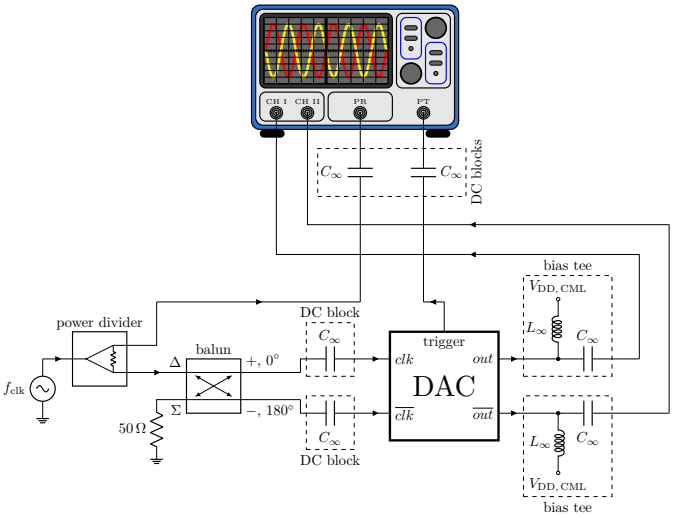
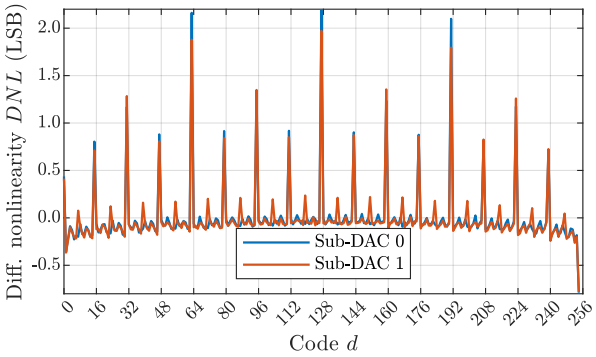
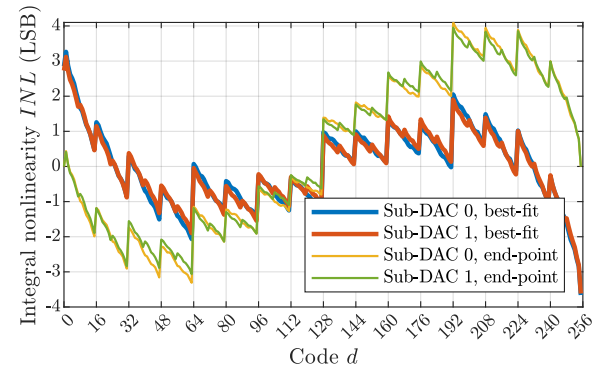


Fig. 15. Measurement setup (PR: phase reference, PT: prescale trigger).



(a)



(b)

Fig. 16. Results of the static characterization measured at 50-GS/s sub-DAC operation corresponding to 100-GS/s operation with activated AMUX. (a) DNL and (b) INL.

line according to IEEE standard [3]. The differential full-scale amplitude is about 0.74 V. In both the DNL and the INL steps with code differences of $\Delta d = 16$ can be observed. These steps appear at the transistions from the R-$2R$ to the unary part and can therefore be attributed to deviations between both parts. However, for the sought application as transmitter at highest data rates these steps are negligible. Neglecting the spikes in the DNL, a weakly pronounced arc is visible in the DNL with minor drops to the outer codes $d = 0$ and $d = 255$ and a deviation of <0.25 LSB. This can be explained by a slight nonlinearity of the output transistors' resistances R_o even if operated in the linear region. Hence, an output voltage dependency is observed. As the transistor widths of the output inverters are designed for an average output voltage of 0.5 V ($d = 127$, $d = 128$), the deviations increase to the corners $d = 0$ and $d = 255$, respectively. However, it has negligible influence on the DNL. The insignificance of this effect confirms the aforementioned choice of the output inverters dimensions in the sub-DACs. In addition, the INL shows limiting behavior. The analysis reveals close matching of the two sub-DACs.

C. Dynamic Characterization by Single-Tone Signals

In Fig. 17, signal-to-noise ratio SNR, signal-to-noise and distortion ratio $SNDR$, signal-to-distortion ratio SDR and spurious free dynamic range $SFDR$ for single-tone signals according to IEEE standard [3] are shown at $f_\mathrm{s} = 64\,\mathrm{GS/s}$ and $f_\mathrm{s} = 100\,\mathrm{GS/s}$. To separate the signal part and distortions from pure random noise, an averaged (x_SD) and a non-averaged time-domain measurement is performed and the noise part (x_N) is determined by subtracting the two measurements. Owing to this method, quantization noise is not included in the SNR values but in $SNDR$. To indicate the exclusion of quantization noise, SNR is marked as $\widehat{SNR}$ in the following. An $SNDR > 28\,\mathrm{dB}$ at $f_\mathrm{s} = 64\,\mathrm{GS/s}$ and an $SNDR > 18\,\mathrm{dB}$ at $f_\mathrm{s} = 100\,\mathrm{GS/s}$ can be determined up to Nyquist frequency. The effective number of bits $ENOB$ is calculated by (6).

$$ENOB \approx \frac{SNDR - 1.76\,\mathrm{dB}}{6.02\,\mathrm{dB}}\,\mathrm{bit} \tag{6}$$

The results are determined by taking an FFT of the output samples captured by the oscilloscope across one data period. At higher signal frequencies, $SNDR$ is limited by increasing distortions due to time-varying effects as well as signal damping and decreases according to the amplitude drop. It becomes obvious that the $SNDR$ is limited by distortions due to the significant similarity between $SNDR$ and SDR. The circuit topology in the sub-DACs which is based on static CMOS logic causes high dynamic load variations and thus supply voltage stability is much more challenging than in approaches with constant currents. The influence of the sub-DAC cores' clock paths on the analog output signals' hold times can explain the investigated spurious components as it generates periodically time-varying artefacts yielding in distortions [51]–[54] which is discussed below. The limitation in $SNDR$ and SDR can essentially be attributed to such kind of distortions and could be reduced by more on-chip supply voltage block capacitance.

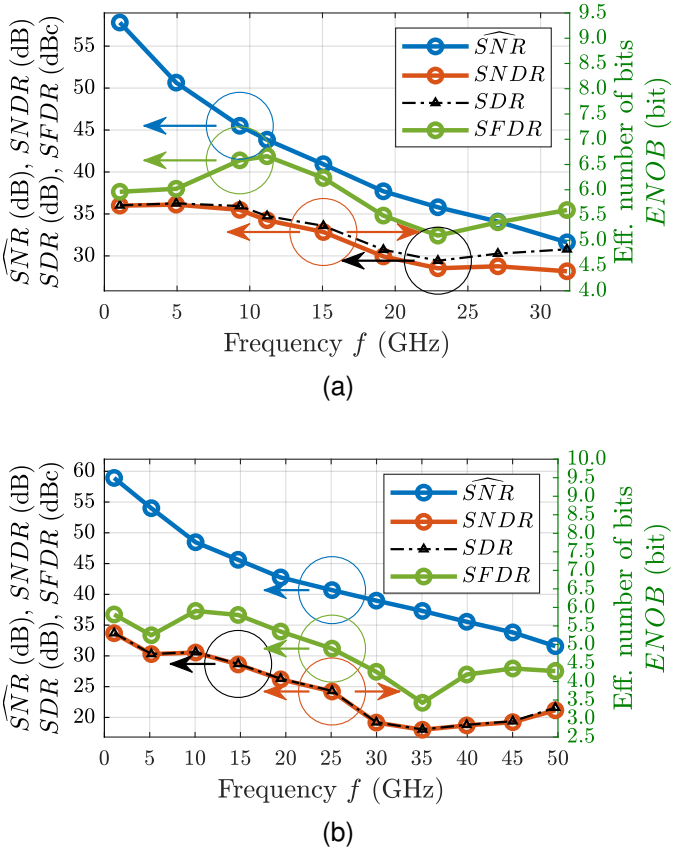


Fig. 17. Dynamic characterization results at (a) 64 GS/s and (b) 100 GS/s.

In the measurements, a partial correction of these distortions using an LPTV filter is already applied.

In Fig. 18, two spectra at $f_\mathrm{s} = 100\,\mathrm{GS/s}$ operation for two signal frequencies $f_\mathrm{sig} \approx 1\,\mathrm{GHz}$ and $f_\mathrm{sig} \approx 50\,\mathrm{GHz}$ are given. The spectra reveal distortions around fractions of the sampling frequency that are predominant, especially at $f_\mathrm{s}/8$ and $f_\mathrm{s}/4$. These distortions can be attributed to deterministic LPTV effects [45]–[48]. In [51]–[54], the impacts of nonuniform holding times on the output spectra of DACs are described and considered as timing mismatch or jitter, respectively. Mirror images around f_s/P can be shown analytically as a consequence of LPTV effects with period P. Furthermore, periodic gain mismatches lead to similar results. Deterministic, periodic effects that correlate with clock network frequencies indicate that predominant distortions arise from clock network artifacts. Considering the MUX tree in Fig. 7a, clock variations have direct impact on the output signal due to the sampling in the last MUX stage. Periodic variations caused by supply voltage load patterns affect the MUX outputs in terms of periodic jitter, i.e. hold time variations, as well as by gain variations and hence the analog output signal in total. Major distortions around $f_\mathrm{s}/8$ and $f_\mathrm{s}/4$ show that the distortions are essentially caused by the sub-DACs due to their CMOS implementation with high dynamic supply voltage load rather than the AMUX. To conclude, the time interleaving by the AMUX is not limiting the performance parameters of this DAC.

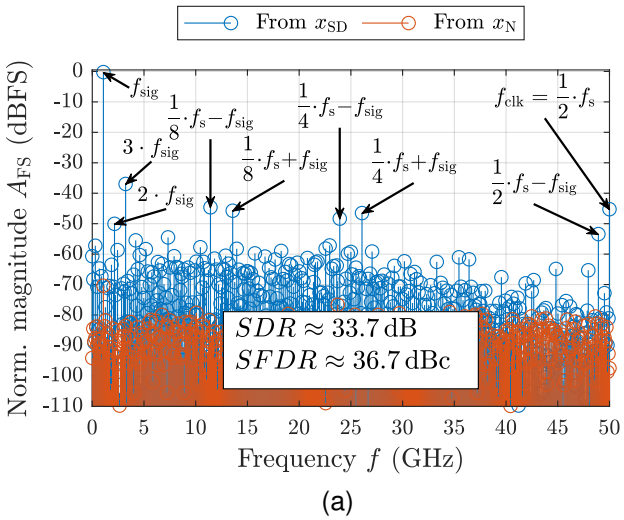


Fig. 18. Spectra normalized to full-scale (FS) at $f_s = 100\,\mathrm{GS/s}$ operation for two signal frequencies (a) $f_{sig} = 1.074218750\,\mathrm{GHz}$ and (b) $f_{sig} = 49.707031250\,\mathrm{GHz}$.

Finally, clock feed-through is also visible.

D. Output Bandwidth

The determination of the output bandwidth is based on three methods according to [3]: sine-wave magnitudes of single-tone measurements at different frequencies, response to an impulse as well as extraction from the derivative of the full-scale step-response. Fig. 19 summarizes the results of these measurements for bandwidth estimation. All mentioned components (bond wires, RF PCB, connectors, cables and bias tees) from chip to the sampling module are included. From single-tone measurements, a −3-dB bandwidth of about 11 GHz can be estimated. On the other side, the impulse and step response measurements reveal a −3-dB bandwidth of about 16 GHz. The bandwidth drop can essentially be attributed to assembly. Bond wires in combination with pad capacitance and technologically limited bandwidth of the RF PCB output

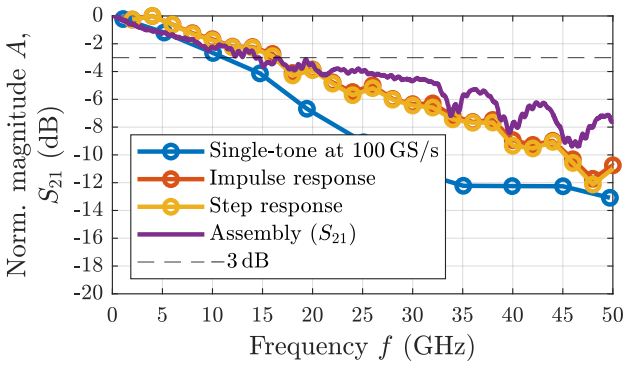


Fig. 19. Bandwidth estimation based on measurements at $f_s = 100\,\mathrm{GS/s}$. The $\sin(x)/x$ roll-off is compensated.

lines limit the −3-dB bandwidth to these values and therefore limit the system performance below the expected real chip performance. As reference, a structure consisting of two replicas of the output line on the RF board connected by bond wires of comparable length to the chip connection is investigated and the result is appended to Fig. 19. The similarity between the overall system's transfer function and the transmission coefficient S_{21} supports the assumption of dominating bandwidth limitations by assembly. However, for broadband signal applications such as the generation of PAM signals, a slow magnitude descent is more important than the value of the −3-dB bandwidth due to predistortion in the whole first Nyquist interval. An attenuation of −10 dB at >45 GHz considering the step response is highly competitive to the CMOS DAC reported in [55] with a −10 dB bandwidth of ∼40 GHz including the $\sin(x)/x$ roll-off. In [2], a commercial 90-GS/s CMOS DAC shows an analog bandwidth of about 19 GHz.

E. PAM Signals

Furthermore, time-domain modulation experiments are investigated. For measurement reasons, a double eye has to be considered as the phase reference is driven by $f_{clk} = f_s/2$. Eye diagrams of broadband PAM signals up to Nyquist frequency without oversampling are depicted in Fig. 20a to Fig. 20g. At 80 GS/s, a PAM-8 signal with 80 GBaud is achieved corresponding to a data rate of 240 Gbit/s. Moreover, at 100 GS/s, PAM-2 and PAM-4 eye diagrams are shown with data rates of 100 Gbit/s and 200 Gbit/s. The highest sampling rate for a signal occupying the whole first Nyquist zone is 108 GS/s for a PAM-2 signal. At higher sampling rates, signal bandwidth has to be reduced. As an example, raised-cosine pulse shaping (roll-off factor 0.5) of an oversampled signal is demonstrated at 118 GS/s in Fig. 20h revealing system operation at sampling rates well beyond 100 GS/s. The corresponding spectrum is shown in Fig. 20i. Figures 20a to 20e, 20g and 20h show eye diagrams for pattern lengths of 1024 (including oversampling in Fig. 20h). A quaternary pseudorandom binary sequence of length 8192 (QPRBS-13) at 100 GS/s is shown in Fig. 20f. It is measured in a different setup than the one of Fig. 20e with slightly reduced signal levels

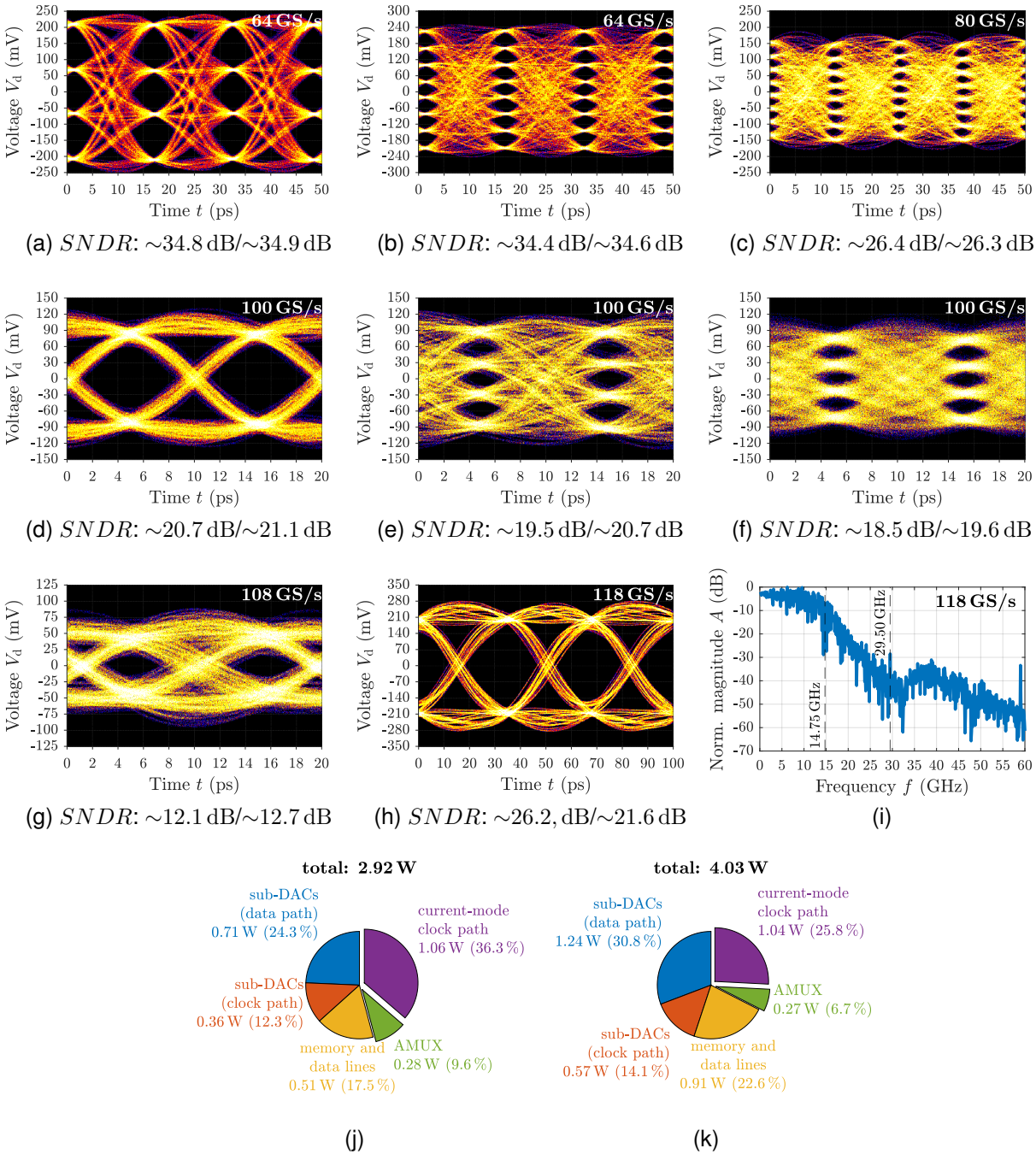


Fig. 20. Measured PAM eye diagrams (differential signals). (a) 64 GS/s PAM-4, (b) 64 GS/s PAM-8, (c) 80 GS/s PAM-8, (d) 100 GS/s PAM-2, (e) 100 GS/s PAM-4, (f) 100 GS/s QPRBS-13, (g) 108 GS/s PAM-2 and (h) 118 GS/s PAM-2 with oversampling and raised-cosine pulse shaping (roll-off factor $\beta = 0.5$). In (i), the spectrum of the signal in (h) is shown. Power breakdowns at 64 GS/s and 100 GS/s are depicted in (j) and (k), respectively. Finally, $SNDR$ values are given for both eye openings.

causing the $SNDR$ values being reduced by approximately 1 dB compared to Fig. 20e. In the measurements, linear predistortion is applied. A quantitative analysis of the eye openings is given by $SNDR$ values determined using the histograms. In case of a PAM-2 signal at $f_s = 100$ GS/s, an $SNDR$ improvement of about 7 dB is reached by LPTV predistortion compared to LTI predistortion with constant (mean) filter coefficients. Power breakdowns for 64 GS/s and 100 GS/s including all losses in external supply lines are given in Fig. 20j and 20k separated into CMOS and current-mode parts as well as into functional blocks. The AMUX power consumption includes source followers at its data inputs. Apparently, the flexible, broadband clock path circuit is an essential part of the overall power consumption. The plots confirm the expected behavior of strong frequency dependency in the CMOS parts and constant power consumption in the current-mode parts. At 118 GS/s, the total power consumption is 5.31 W.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART CMOS REALIZATIONS.

Reference	TMTT 2015 [12]	BCICTS 2019 [56]	ISSCC 2020 [57]	ISSCC 2021 [58]	ISSCC 2021 [39]/ JSSC 2022 [40]	JSSC 2023 [35]	This work
Technology	28 nm	7 nm	7 nm	7 nm	10 nm	4 nm	28 nm
System (memory)	AWG (1 kB)	AWG (256 B)	Tx	Tx	Tx (optional)	Tx (32 kB)	AWG (256 kB)
Architecture	Half-rate[e]	Half-rate	Half-rate	Quarter-rate	Quarter-rate	Quarter-rate	Half-rate
Nominal resolution (bit)	8	8	7	8	7	8	8
Sampling rate (GS/s)	100 50 (PAM-4) 40 (PAM-2/4/8)	60	56 (PAM-4)	97	116 (PAM-2/4) 112 (PAM-2/4) 56 (PAM-8)	72 (PAM-2/4/6/8)	118[a] 108 (PAM-2) 100 (PAM-2/4) 80 (PAM-8)
Data rate (Gbit/s)	120 (PAM-8) 100 (PAM-4) 80 (PAM-4) 40 (PAM-2)	-[g]	112 (PAM-4)	132 (PAM-4)	232 (PAM-4) 224 (PAM-4) 168 (PAM-8) 116 (PAM-2) 112 (PAM-2)	216 (PAM-8) ∼186 (PAM-6) 144 (PAM-4) 72 (PAM-2)	240 (PAM-8) 200 (PAM-4) 108 (PAM-2) 100 (PAM-2)
Bandwidth (GHz)	∼13[f]	-	-	∼36	∼36[d]	∼11	∼11[b] -16[c]
Power consumption (W)	2.5	0.56	0.175	0.308 (Tx)	0.423 (analog) 0.083 (FFE)	0.288	4.03 (@ 100 GS/s)
Efficiency	25 pJ/bit (@ 50 GS/s, PAM-4)	-	1.56 pJ/bit (@ 56 GS/s, PAM-4)	90.2 fJ/c-s (@ 30 GHz, w/o PLL)	1.88 pJ/bit (analog) 0.37 pJ/bit (FFE) (@ 112 GS/s, PAM-4)	2 pJ/bit (@ 72 GS/s, PAM-4)	20.2 pJ/bit (@ 100 GS/s, PAM-4) 15.6 pJ/bit (w/o memory)
Supply voltages (V)	-	0.9/1.9	0.9/1.2	1.8	0.85/1/1.5	0.95	1/1.6/ −1.3/ − 0.6
Max. output swing (V_{ppd})	1	0.8	1.2	1.1	1.0	0.92	0.74
$SNDR$ (dB)	∼21.0 dB (min., @ 100 GS/s)	∼29.5 dB (min., @ 60 GS/s)	-	∼32.76 dB (@ 30 GHz)	∼33.3 dB (@ 112 GS/s, PAM-4)	∼27.3 dB (@ 13.46 GHz)	∼18 dB (min., @ 100 GS/s)
Area	1.6 mm ×0.9 mm = 1.44 mm^2	0.62 mm ×0.50 mm = 0.31 mm^2 (DAC core, excluding memory)	0.193 mm^2	2.35 mm^2 (4 Tx + PLL)	0.088 mm^2 (excluding PLL, pattern generator, memory, DSP)	1.328 mm ×1.420 mm ≈ 1.89 mm^2 (Tx core: 215.7 µm ×219.8 µm)	1.692 mm ×1.692 mm ≈ 2.86 mm^2 (including memory) (sub-DAC core: ∼215 µm ×100 µm)

[a] oversampling, pulse shaping [b] from single-tone measurement, −3 dB [c] from impulse/step response, −3 dB [d] measurement of packaging only, −3 dB [e] in sub-DACs [f] RF probe [g] 56 Gbit/s (PAM-2) with former chip in 65 nm CMOS [59]

VI. COMPARISON TO THE STATE OF THE ART

A comparison to a selection of state-of-the-art DACs in DAC-based Tx front-ends for ultra-high-speed wireline applications as well as to AWGs is summarized in Table I. It becomes obvious that in terms of sampling rate and data rate, previous data is outperformed in at least one of these parameters despite bandwidth limitation and larger CMOS node. This shows that the concept of an integrated AMUX is a powerful concept for DAC performance enhancement. Sampling rates well above 100 GS/s are possible. Moreover, this circuit features full, stand-alone AWG functionality due to on-chip memory that is much larger than test memories in Tx systems. The main performance limitation is given by the bandwidth limitation mainly caused by assembly underestimating the true DAC performance and hence, it is not a conceptual one. For the sake of completeness, a 120-GS/s DAC in 16-nm CMOS is mentioned in [55] and used in an optical transmission system to generate 105-GBaud signals. A comparison to the best performing AWGs in BiCMOS technology with SiGe heterojunction bipolar transistors operating at 100 GS/s [4], 128 GS/s [5] and 134 GS/s [6] reveals that the concept of an integrated AMUX is also able to decrease the gap between bipolar approaches and CMOS solutions in terms of sampling rates. Considering the power consumptions of 15 W and 18 W for the BiCMOS AWGs in [4] and [5], a CMOS AWG has still remarkable advantage over BiCMOS in that point.

VII. CONCLUSION

To conclude, two sub-DACs with time interleaving in the analog domain by active, analog multiplexing are shown being capable of pushing the sampling rates of CMOS DACs clearly

beyond $100\,\mathrm{GS/s}$. An additional on-chip memory of $256\,\mathrm{kB}$ completes the system to an AWG. In the sub-DACs with CMOS inverter-based output concept, resistive feedback is used in the output stages and in the clock network. There, a different trade-off between bandwidth and gain is chosen and a feedback across three inverters is used to optimize performance at less static power consumption compared to the concept in the output stages with feedback across one inverter. The sub-DAC concept does not require transistor stacking and is more amenable to integration in highly integrated digital circuits [35]. In general, DAC-based SST transmitter approaches are of special interest for wireline applications [35]. However, it causes large dynamic loads that might cause spurious components and therefore requires appropriate on-chip decoupling capacitance. To further improve performance, more on-chip decoupling capacitance is required to reduce periodic distortions according to the clock network. Moreover, constant loading concepts as presented in [60] might reduce data-dependent distortions. In terms of sampling or data rates, other state-of-the-art concepts can be exceeded in at least one of these parameters despite a larger CMOS node of $28\,\mathrm{nm}$. As predistortion, an LPTV predistortion is applied using a two-dimensional LUT for the periodically changing filter coefficients. As the concept may be applied to any given DAC architecture, power consumption can be reduced by different sub-DAC and clock path architectures as it is dominated by these circuit parts. As clock path architecture, quarter-rate or narrowband resonant concepts could reduce power consumption. In combination with more complex high-bandwidth packaging technologies such as flip-chip, even higher performance parameters could potentially be achieved. The demonstrated sampling rates show the potential of the concept using an integrated AMUX.

Acknowledgment

We thank Wolfgang Templ, Fred Buchali and Peter Klose from Nokia Bell Labs and Nokia Stuttgart for their extensive support in the complex packaging of this integrated circuit.

References

[1] F. Buchali, "Beyond 1 Tbit/s transmission using high-speed DACs and analog multiplexing," in *2021 Optical Fiber Communications Conference and Exhibition (OFC)*, 2021.

[2] C. Schmidt *et al.*, "120 GBd SiGe-Based 2:1 Analog Multiplexer Module for Ultra-Broadband Transmission Systems," in *2021 16th European Microwave Integrated Circuits Conference (EuMIC)*, 2022, pp. 169–172.

[3] "IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices," *IEEE Std 1658-2011*, 2012.

[4] K. Schuh *et al.*, "100 GSa/s BiCMOS DAC Supporting 400 Gb/s Dual Channel Transmission," in *ECOC 2016; 42nd European Conference on Optical Communication*, 2016.

[5] F. Buchali *et al.*, "128 GSa/s SiGe DAC Implementation Enabling 1.52 Tb/s Single Carrier Transmission," *Journal of Lightwave Technology*, vol. 39, no. 3, pp. 763–770, 2021.

[6] F. Pittalà *et al.*, "1.71 Tb/s Single-Channel and 56.51 Tb/s DWDM Transmission Over 96.5 km Field-Deployed SSMF," *IEEE Photonics Technology Letters*, vol. 34, no. 3, pp. 157–160, 2022.

[7] E. Olieman, A.-J. Annema, and B. Nauta, "An Interleaved Full Nyquist High-Speed DAC Technique," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 3, pp. 704–713, 2015.

[8] S. Balasubramanian *et al.*, "Systematic Analysis of Interleaved Digital-to-Analog Converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 12, pp. 882–886, 2011.

[9] C. Schmidt, *Interleaving Concepts for Digital-to-Analog Converters – Algorithms, Models, Simulations and Experiments*, 1st ed. Wiesbaden: Springer Vieweg, 2020.

[10] J. Deveugele, P. Palmers, and M. Steyaert, "Parallel-Path Digital-to-Analog Converters for Nyquist Signal Generation," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1073–1082, 2004.

[11] H. Hettrich, R. Schmid, L. Altenhain, J. Würtele, and M. Möller, "A Linear Active Combiner Enabling an Interleaved 200 GS/s DAC with 44 GHz Analog Bandwidth," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2017, pp. 142–145.

[12] H. Huang *et al.*, "An 8-bit 100-GS/s Distributed DAC in 28-nm CMOS for Optical Communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1211–1218, 2015.

[13] T. Tannert *et al.*, "A SiGe-HBT 2:1 Analog Multiplexer with more than 67 GHz Bandwidth," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2017, pp. 146–149.

[14] K. Schuh *et al.*, "100 GSa/s BiCMOS Analog Multiplexer Based 100 GBd PAM Transmission over 20 km Single-Mode Fiber in the C-Band," in *2020 European Conference on Optical Communications (ECOC)*, 2020.

[15] M. Collisi and M. Möller, "A 120 GS/s 2:1 Analog Multiplexer with High Linearity in SiGe-BiCMOS Technology," in *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2020.

[16] J. Schostak *et al.*, "150 GBd PAM-4 Electrical Signal Generation using SiGe-Based Analog Multiplexer IC," in *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*, 2022, pp. 173–176.

[17] R. Hersent *et al.*, "160-GSa/s-and-Beyond 108-GHz-Bandwidth Over-2-Vppd Output-Swing 0.5-µm InP DHBT 2:1 AMUX-Driver for Next-Generation Optical Communications," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 752–755, 2022.

[18] M. Nagatani *et al.*, "A 110-GHz-Bandwidth 2:1 AMUX-Driver using 250-nm InP DHBTs for Beyond-1-Tb/s/carrier Optical Transmission Systems," in *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2019.

[19] ——, "A Beyond-1-Tb/s Coherent Optical Transmitter Front-End Based on 110-GHz-Bandwidth 2:1 Analog Multiplexer in 250-nm InP DHBT," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2301–2315, 2020.

[20] H. Ramon *et al.*, "12.4 A 700mW 4-to-1 SiGe BiCMOS 100GS/s Analog Time-Interleaver," in *2020 IEEE International Solid-State Circuits Conference (ISSCC)*, 2020, pp. 214–216.

[21] ——, "A 100-GS/s Four-to-One Analog Time Interleaver in 55-nm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2539–2549, 2021.

[22] P. Caragiulo, O. E. Mattia, A. Arbabian, and B. Murmann, "A 2× Time-Interleaved 28-GS/s 8-Bit 0.03-mm^2 Switched-Capacitor DAC in 16-nm FinFET CMOS," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2335–2346, 2021.

[23] A. Cathelin, "Fully Depleted Silicon on Insulator Devices CMOS: The 28-nm Node Is the Perfect Technology for Analog, RF, mmW, and Mixed-Signal System-on-Chip Integration," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 18–26, 2017.

[24] S. Clerc, T. Di Gilio, and A. Cathelin, Eds., *The Fourth Terminal: Benefits of Body-Biasing Techniques for FDSOI Circuits and Systems*, ser. Integrated Circuits and Systems. Cham: Springer Nature Switzerland, 2020.

[25] S. Shekhar, J. Walling, and D. Allstot, "Bandwidth Extension Techniques for CMOS Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, 2006.

[26] J. S. Walling, S. Shekhar, and D. J. Allstot, "Wideband CMOS Amplifier Design: Time-Domain Considerations," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 7, pp. 1781–1793, 2008.

[27] D. Widmann, T. Tannert, X.-Q. Du, M. Grözing, and M. Berroth, "Multi-Phase Clock Path Circuit up to 57 GHz Including 5 bit Programmable Phase Interpolators for Time-Interleaved Broadband Data Converters in a 28 nm FD-SOI CMOS Technology," in *2021 16th European Microwave Integrated Circuits Conference (EuMIC)*, 2022, pp. 177–180.

[28] J. Deveugele and M. Steyaert, "A 10-bit 250-MS/s Binary-Weighted Current-Steering DAC," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 320–329, 2006.

[29] X. Wu, P. Palmers, and M. S. J. Steyaert, "A 130 nm CMOS 6-bit Full Nyquist 3 GS/s DAC," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2396–2403, 2008.

[30] M. Ingels, G. Van Der Plas, J. Crols, and M. Steyaert, "A CMOS 18 THzΩ 240 Mb/s Transimpedance Amplifier and 155 Mb/s LED-driver

for Low Cost Optical Fiber Links," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1552–1559, 1994.

[31] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, "CMOS Wideband Amplifiers Using Multiple Inductive-Series Peaking Technique," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 548–552, 2005.

[32] S.-F. Chao, J.-J. Kuo, C.-L. Lin, M.-D. Tsai, and H. Wang, "A DC-11.5 GHz Low-Power, Wideband Amplifier Using Splitting-Load Inductive Peaking Technique," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 7, pp. 482–484, 2008.

[33] C. Menolfi *et al.*, "A 16Gb/s Source-Series Terminated Transmitter in 65nm CMOS SOI," in *2007 IEEE International Solid-State Circuits Conference (ISSCC). Digest of Technical Papers*, 2007.

[34] B. Razavi, *Design of Integrated Circuits for Optical Communications*, 1st ed., ser. McGraw-Hill Higher Education. Boston: McGraw-Hill, 2003.

[35] T. O. Dickson *et al.*, "A 72-GS/s, 8-Bit DAC-Based Wireline Transmitter in 4-nm FinFET CMOS for 200+ Gb/s Serial Links," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 4, pp. 1074–1086, 2023.

[36] K. Abugharbieh, S. Krishnan, J. Mohan, V. Devnath, and I. Duzevik, "An Ultralow-Power 10-Gbits/s LVDS Output Driver," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 1, pp. 262–269, 2010.

[37] C. Menolfi *et al.*, "A 112Gb/S 2.6pJ/b 8-Tap FFE PAM-4 SST TX in 14nm CMOS," in *2018 IEEE International Solid-State Circuits Conference (ISSCC)*, 2018, pp. 104–106.

[38] M. A. Kossel *et al.*, "8.3 An 8b DAC-Based SST TX Using Metal Gate Resistors with 1.4pJ/b Efficiency at 112Gb/s PAM-4 and 8-Tap FFE in 7nm CMOS," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, 2021, pp. 130–132.

[39] J. Kim *et al.*, "8.1 A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, 2021, pp. 126–128.

[40] ——, "A 224-Gb/s DAC-Based PAM-4 Quarter-Rate Transmitter With 8-Tap FFE in 10-nm FinFET," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 1, pp. 6–20, 2022.

[41] S. Sidiropoulos and M. Horowitz, "A Semidigital Dual Delay-Locked Loop," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 11, pp. 1683–1692, 1997.

[42] G. Wu *et al.*, "A 1–16 Gb/s All-Digital Clock and Data Recovery With a Wideband High-Linearity Phase Interpolator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 7, pp. 2511–2520, 2016.

[43] R. Kreienkamp, U. Langmann, C. Zimmermann, T. Aoyama, and H. Siedhoff, "A 10-Gb/s CMOS Clock and Data Recovery Circuit With an Analog Phase Interpolator," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 736–743, 2005.

[44] L. Rodoni, G. von Buren, A. Huber, M. Schmatz, and H. Jackel, "A 5.75 to 44 Gb/s Quarter Rate CDR With Data Rate Selection in 90 nm Bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 1927–1941, 2009.

[45] A. Mehr and T. Chen, "Representations of Linear Periodically Time-Varying and Multirate Systems," *IEEE Transactions on Signal Processing*, vol. 50, no. 9, pp. 2221–2229, 2002.

[46] C. Vogel and C. Krall, "Compensation of Distortions Caused by Periodic Nonuniform Holding Signals," in *2008 6th International Symposium on Communication Systems, Networks and Digital Signal Processing*, 2008, pp. 152–155.

[47] S. Pavan and R. S. Rajan, "Interreciprocity in Linear Periodically Time-Varying Networks With Sampled Outputs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 9, pp. 686–690, 2014.

[48] S. Pavan, "On Linear Periodically Time Varying (LPTV) Systems with Modulated Inputs, and their Application to Smoothing Filters," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017.

[49] J. Speidel, *Introduction to Digital Communications*, 2nd ed., ser. Signals and Communication Technology. Cham: Springer Nature Switzerland AG, 2021.

[50] P. A. Bello, "Characterization of Randomly Time-Variant Linear Channels," *IEEE Transactions on Communications Systems*, vol. 11, no. 4, pp. 360–393, 1963.

[51] Y.-C. Jenq, "Digital-to-Analog (D/A) Converters with Nonuniformly Sampled Signals," *IEEE Transactions on Instrumentation and Measurement*, vol. 45, no. 1, 1996.

[52] ——, "Direct Digital Synthesizer with Jittered Clock," *IEEE Transactions on Instrumentation and Measurement*, vol. 46, no. 3, 1997.

[53] S.-P. U, S.-W. Sin, and R. Martins, "Exact Spectra Analysis of Sampled Signals With Jitter-Induced Nonuniformly Holding Effects," *IEEE Transactions on Instrumentation and Measurement*, vol. 53, no. 4, 2004.

[54] L. Angrisani and M. D'Arco, "Modeling Timing Jitter Effects in Digital-to-Analog Converters," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 2, 2009.

[55] F. Buchali, V. Lauinger, M. Chagnon, K. Schuh, and V. Aref, "CMOS DAC Supported 1.1 Tb/s/λ DWDM Transmission at 9.8 bit/s/Hz Over DCI Distances," *Journal of Lightwave Technology*, vol. 39, no. 4, pp. 1171–1178, 2021.

[56] Y. Greshishchev *et al.*, "A 60 GS/s 8-b DAC with $>$ 29.5dB SINAD up to Nyquist frequency in 7nm FinFET CMOS," in *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2019.

[57] E. Groen *et al.*, "6.3 A 10-to-112Gb/s DSP-DAC-Based Transmitter with 1.2Vppd Output Swing in 7nm FinFET," in *2020 IEEE International Solid-State Circuits Conference (ISSCC)*, 2020, pp. 120–122.

[58] R. L. Nguyen *et al.*, "8.6 A Highly Reconfigurable 40-97GS/s DAC and ADC with 40GHz AFE Bandwidth and Sub-35fJ/conv-step for 400Gb/s Coherent Optical Applications in 7nm FinFET," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, 2021, pp. 136–138.

[59] Y. M. Greshishchev *et al.*, "A 56GS/s 6b DAC in 65nm CMOS with 256×6b Memory," in *2011 IEEE International Solid-State Circuits Conference (ISSCC)*, 2011, pp. 194–196.

[60] D. A. Mercer, "Low-Power Approaches to High-Speed Current-Steering Digital-to-Analog Converters in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1688–1698, 2007.

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