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20. Workshop Analogschaltungen

12. – 13. März 2018

Analoge Verzögerungsregelschleife für die digitale HF-Pulsweitenmodulation im Frequenzbereich von 170 MHz bis 2,8 GHz in 28 nm FDSOI CMOS

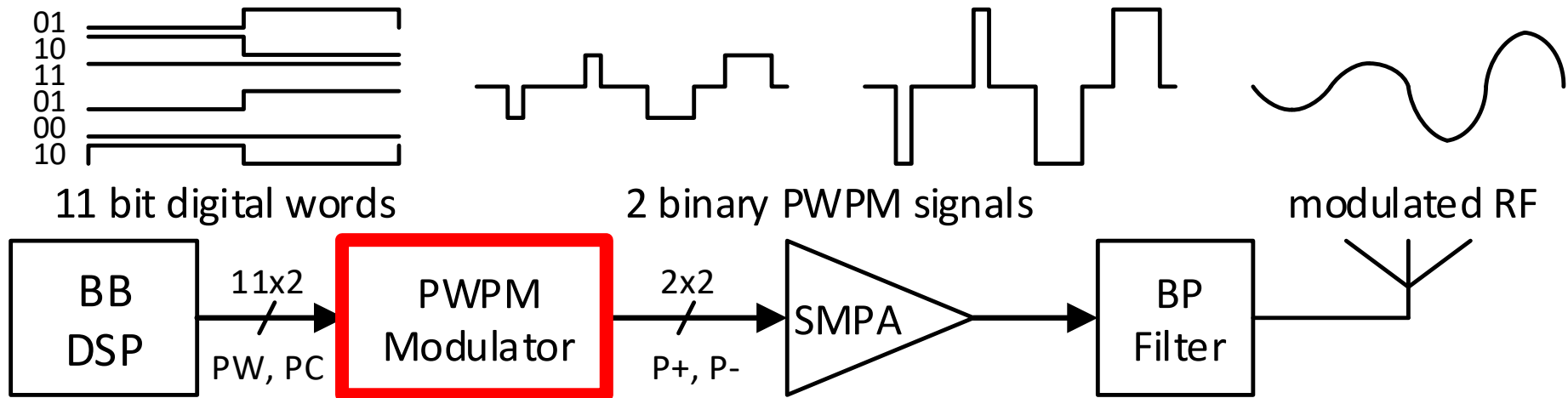
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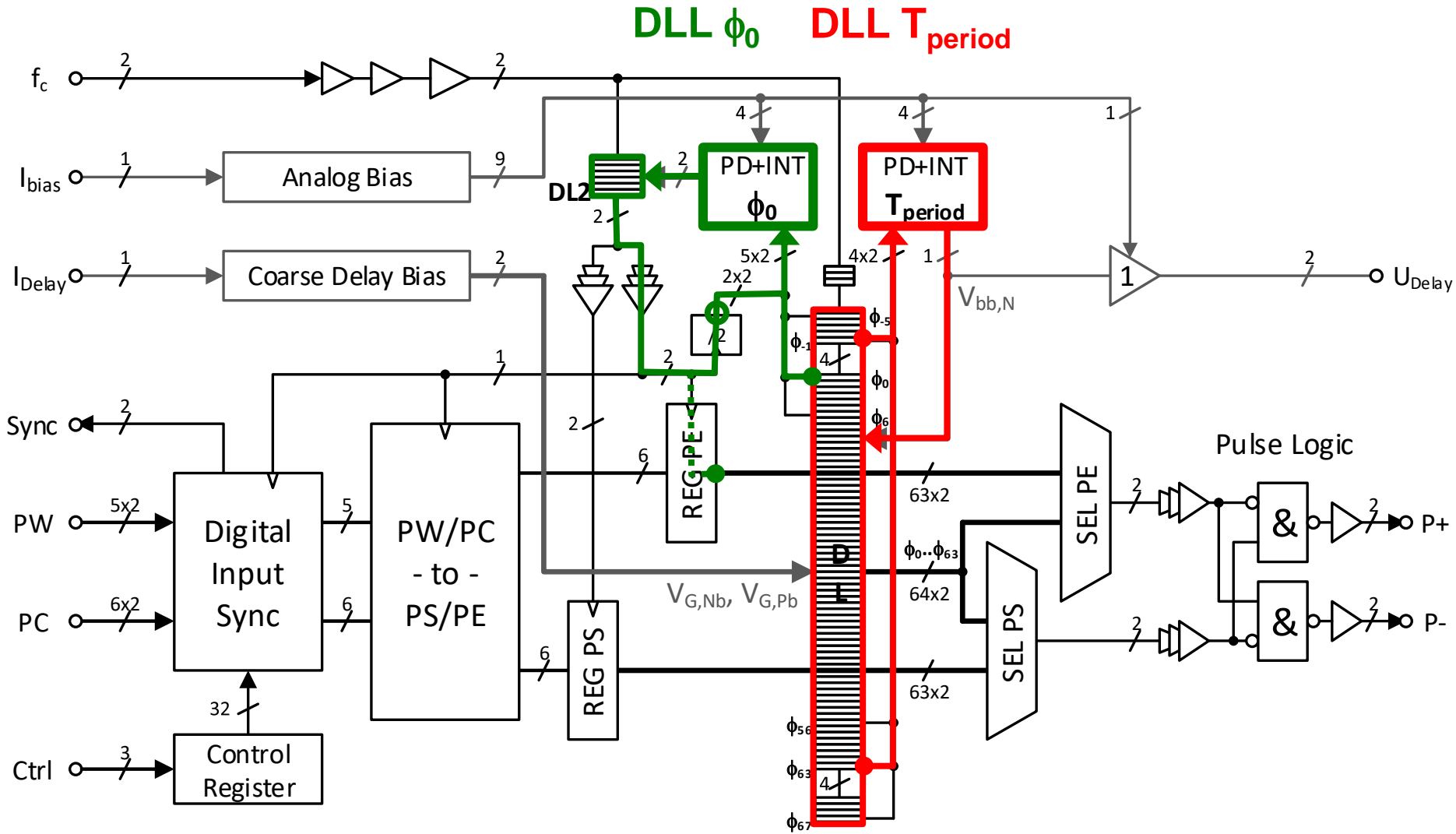
² Nokia Bell Labs, Stuttgart

- Zielanwendung
- Modulatorkonzept
- Schaltungsentwurf Verzögerungsschleife
 - Verzögerungszelle
 - Integrierender Phasedetektor
- Messergebnisse
 - Statische Konstellationsdiagramme
 - Modulierte HF-Signale
- Zusammenfassung
- Referenzen

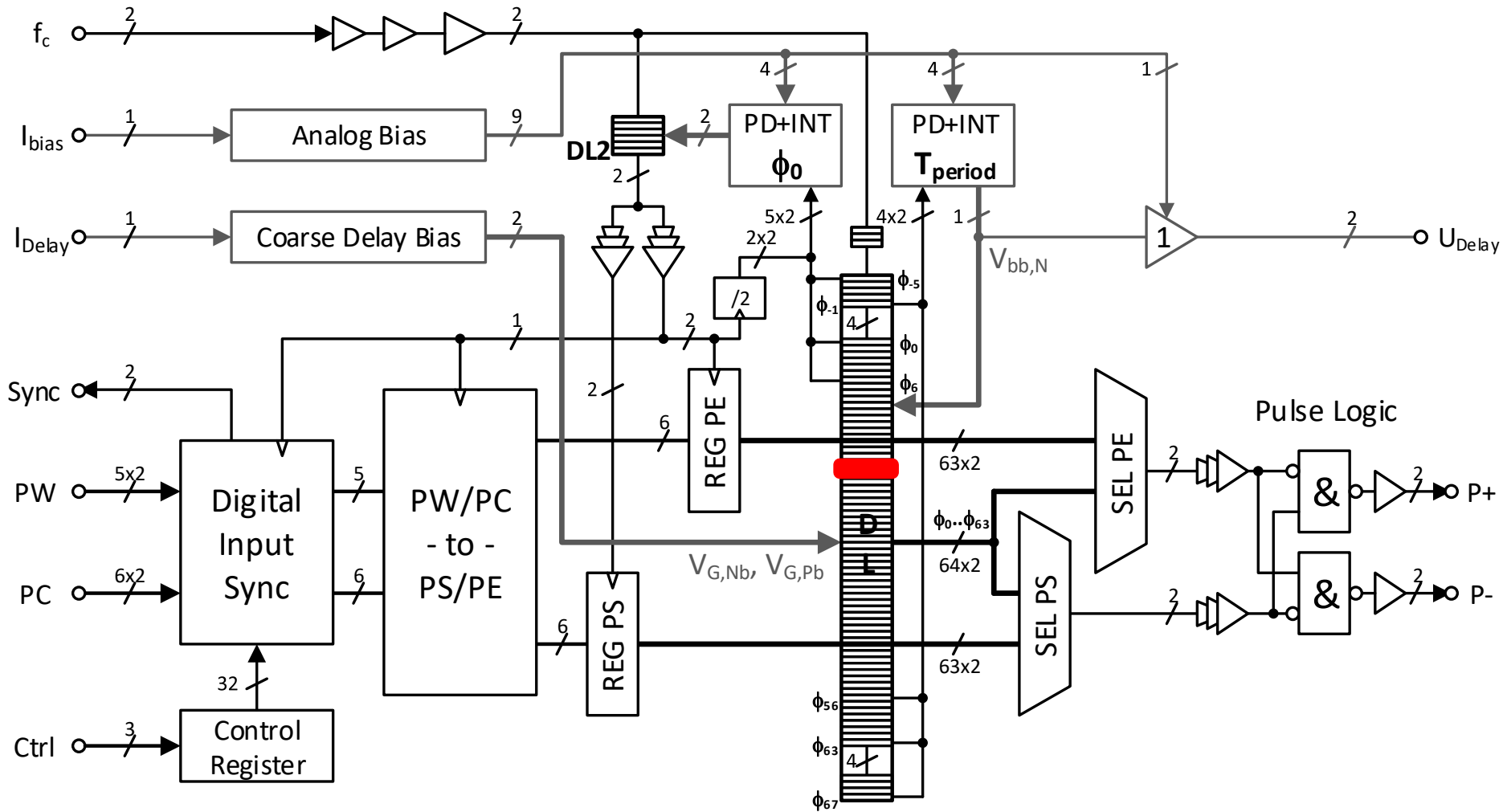
Zielanwendung: HF-Sender mit PPWM und Schaltverstärker



Digitaler Pulspositions- und Pulsweiten-Modulator

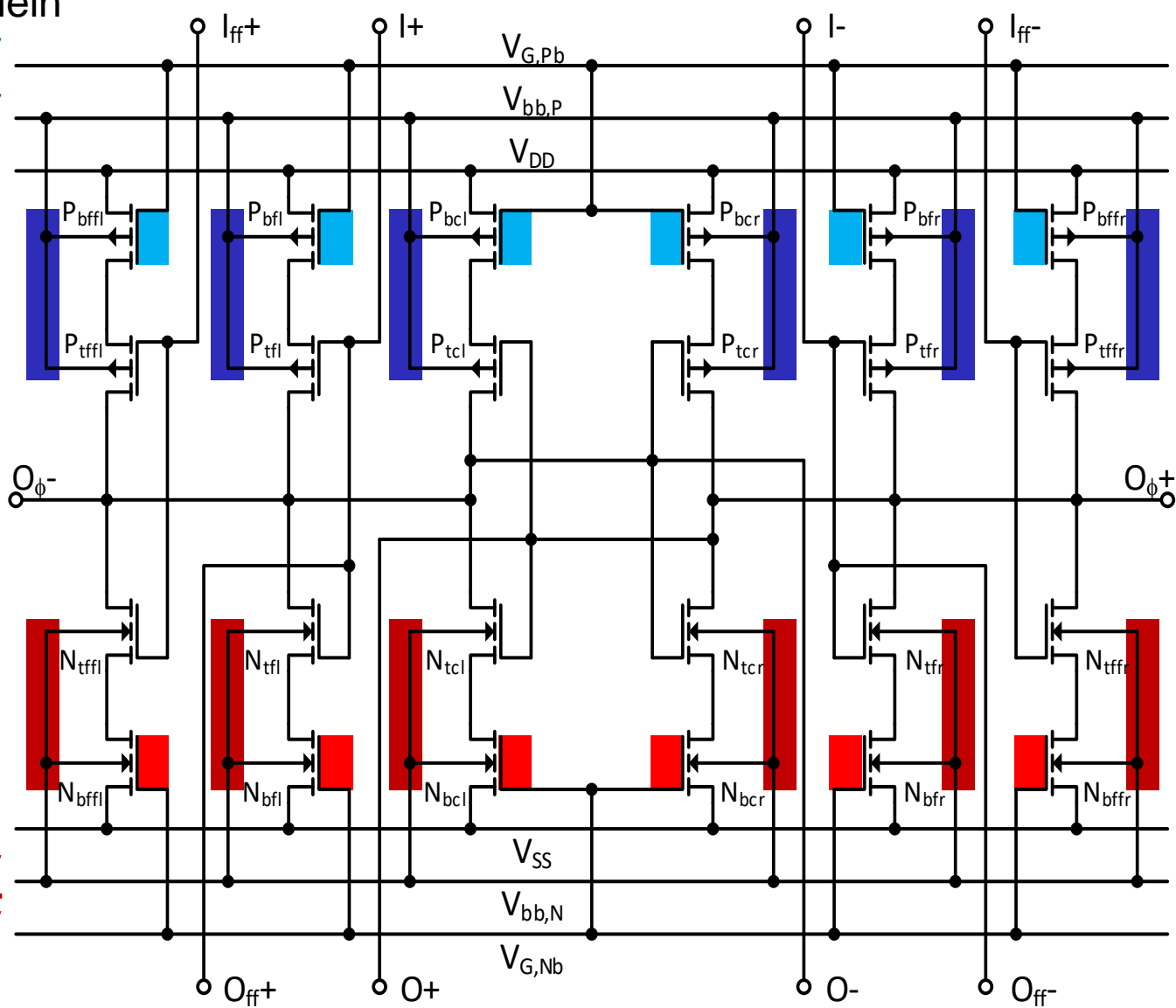


Digitaler Pulspositions- und Pulsweiten-Modulator



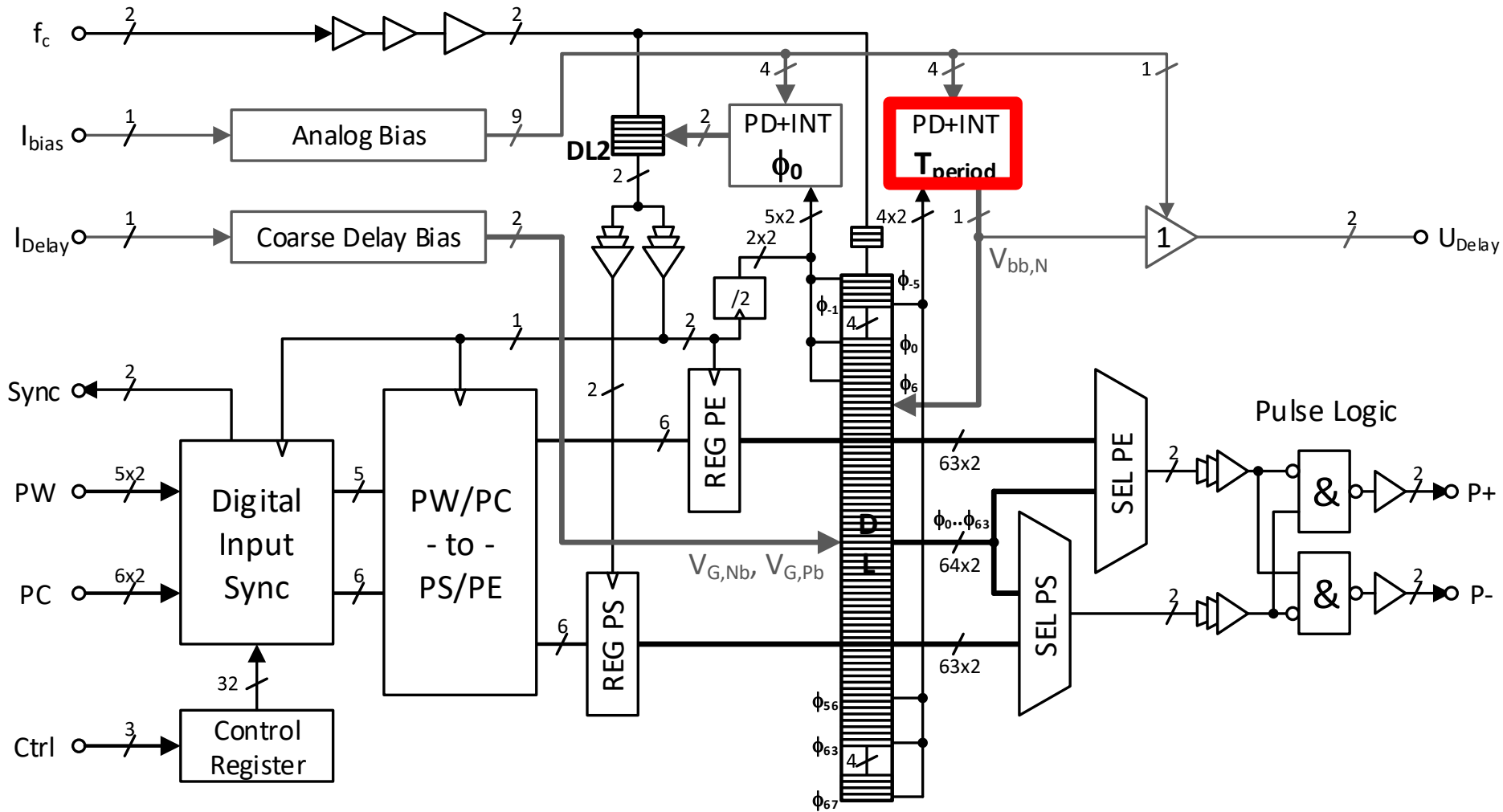
Schaltplan Verzögerungszelle in FDSOI CMOS

Spg. Einst. Δt groß..klein
 $V_{G,Pb}$ **grob** 1V..0V
 $V_{bb,P}$ **fein** 1V..0V
 V_{DD} 1V

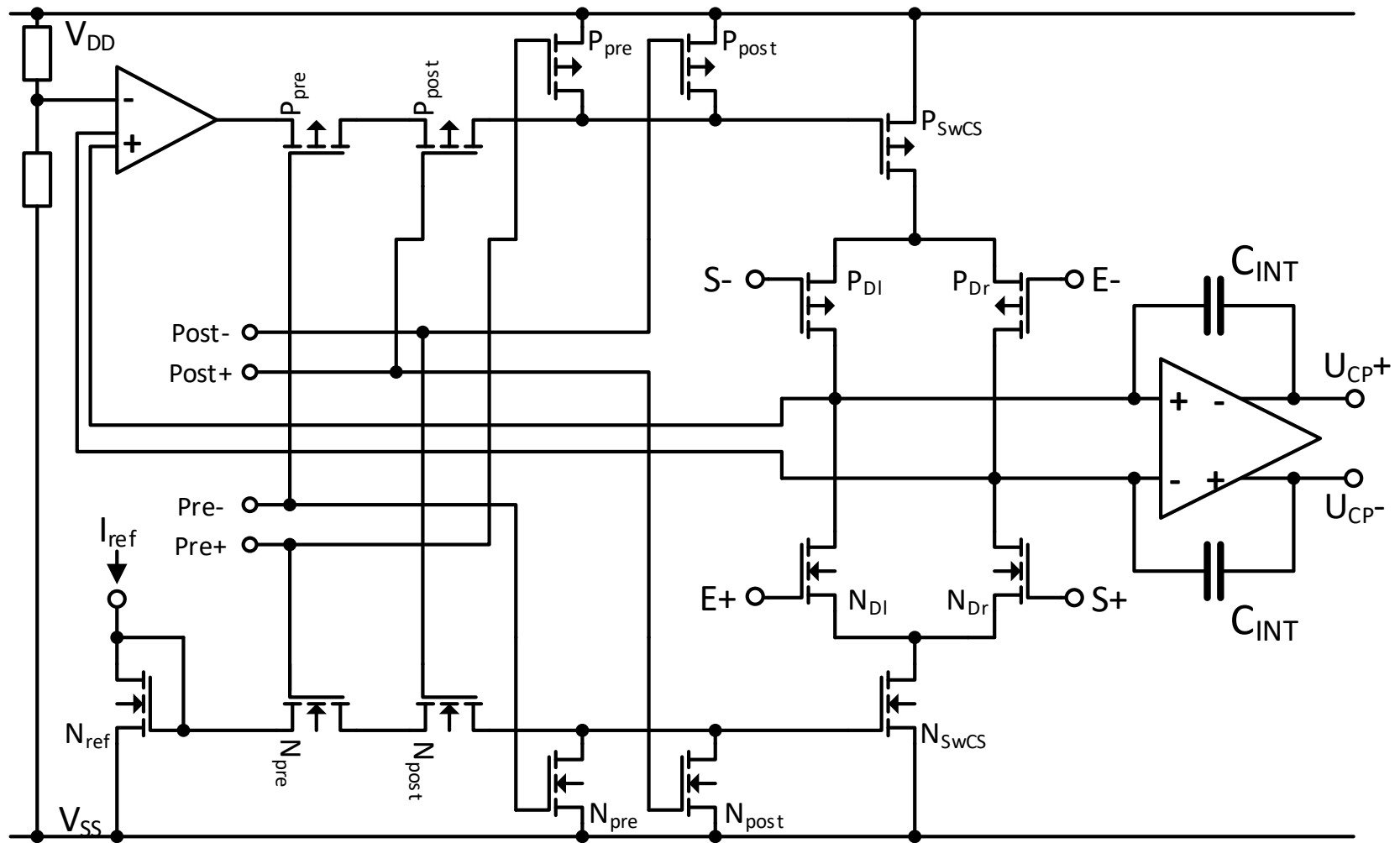


V_{SS} 0 V
 $V_{bb,N}$ **fein** 0V..1V
 $V_{G,Nb}$ **grob** 0V..1V

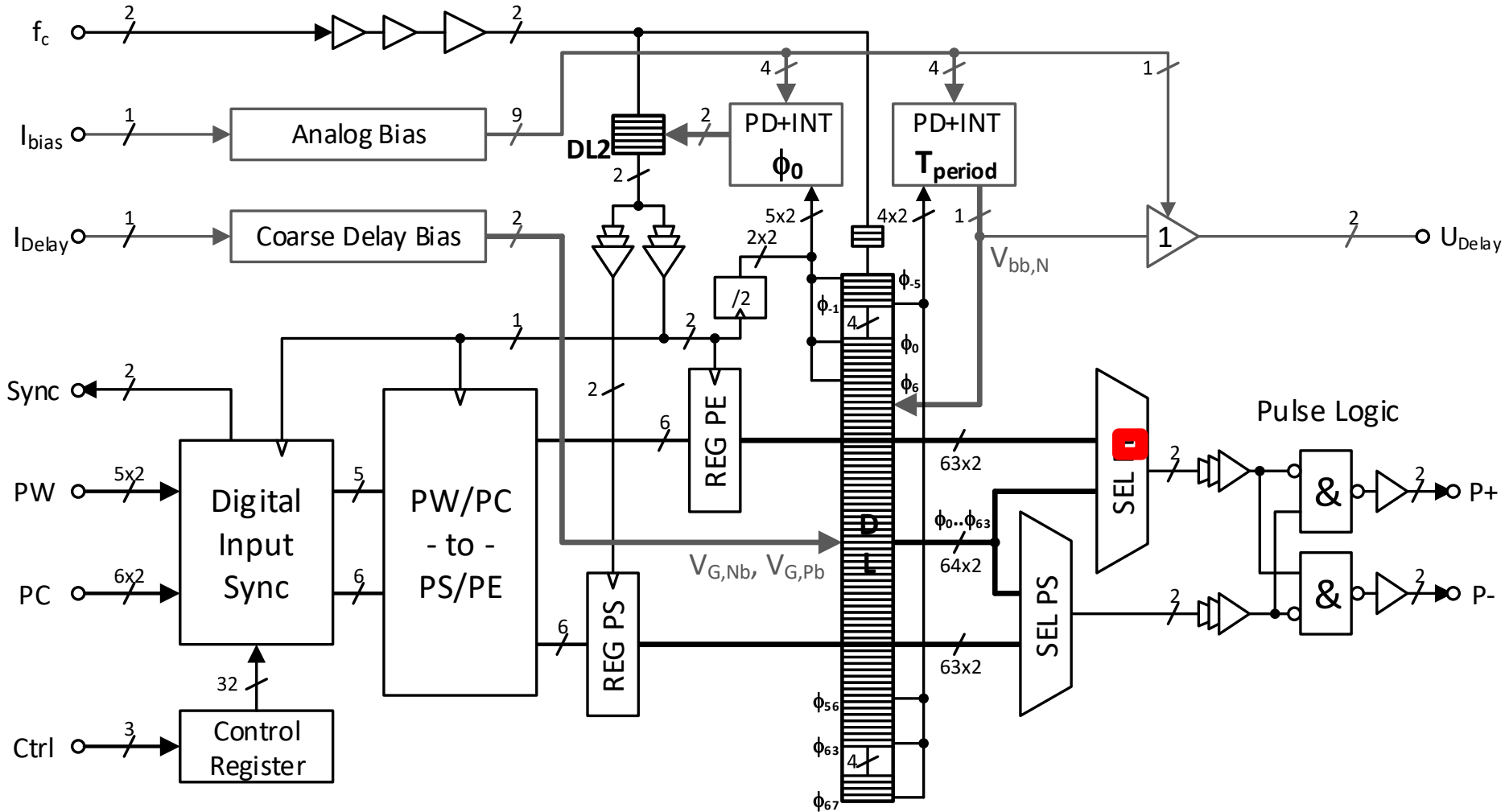
Digitaler Pulspositions- und Pulsweiten-Modulator



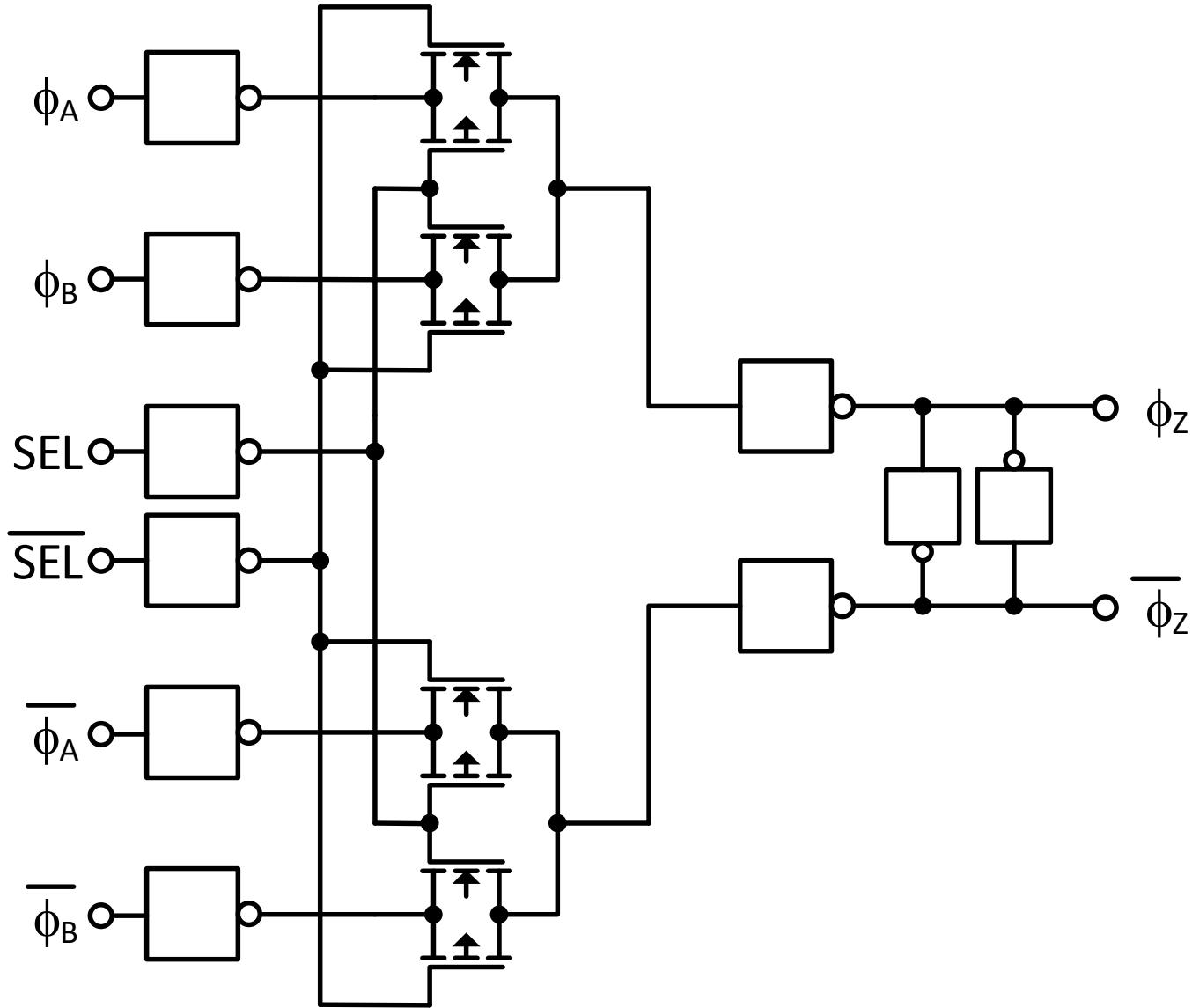
Integrierender Stromschalter-Phasendetektor



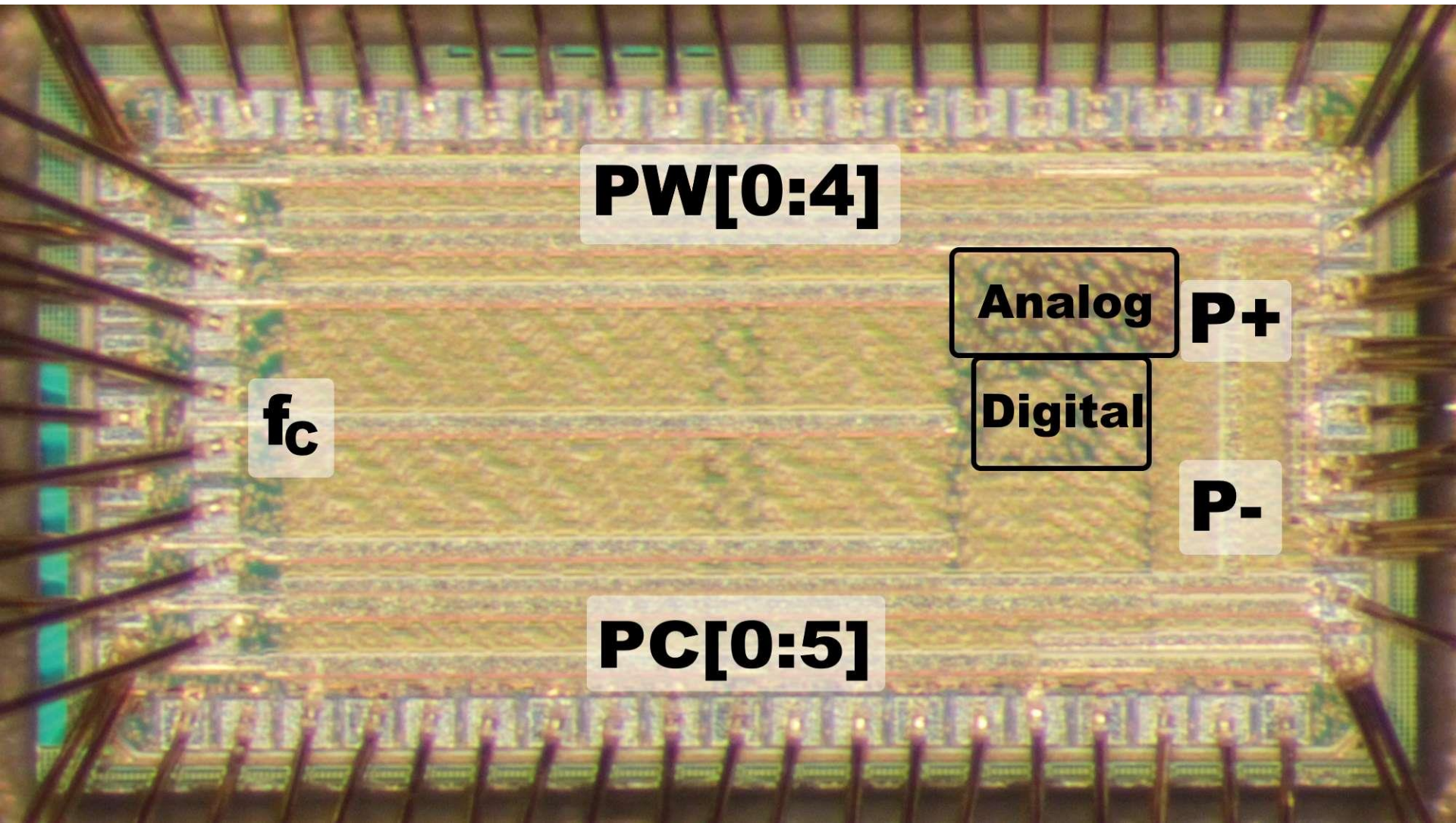
Digitaler Pulspositions- und Pulsweiten-Modulator



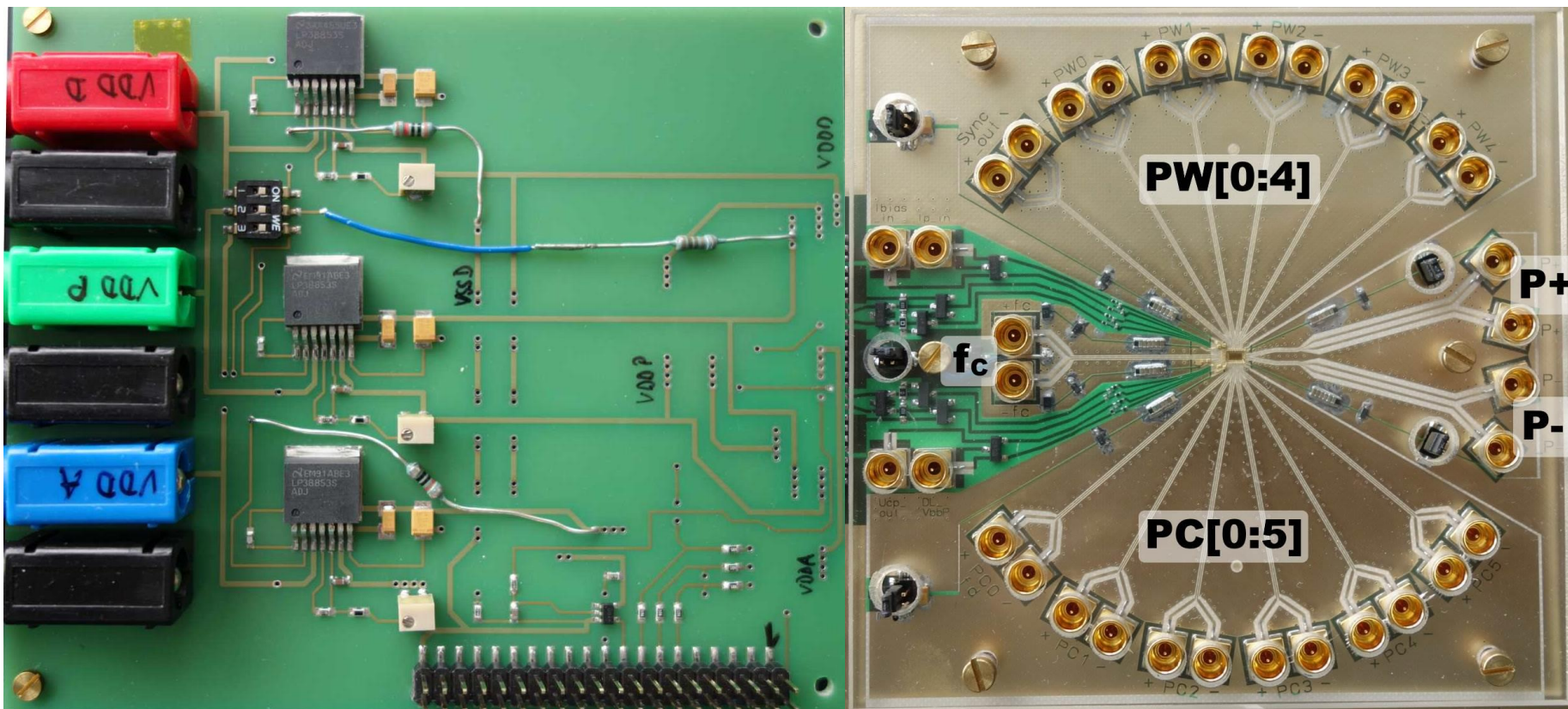
Schaltplan 2-zu-1 Selektor



Chipfoto HF PPWM IC: 1.9 mm x 1.0 mm

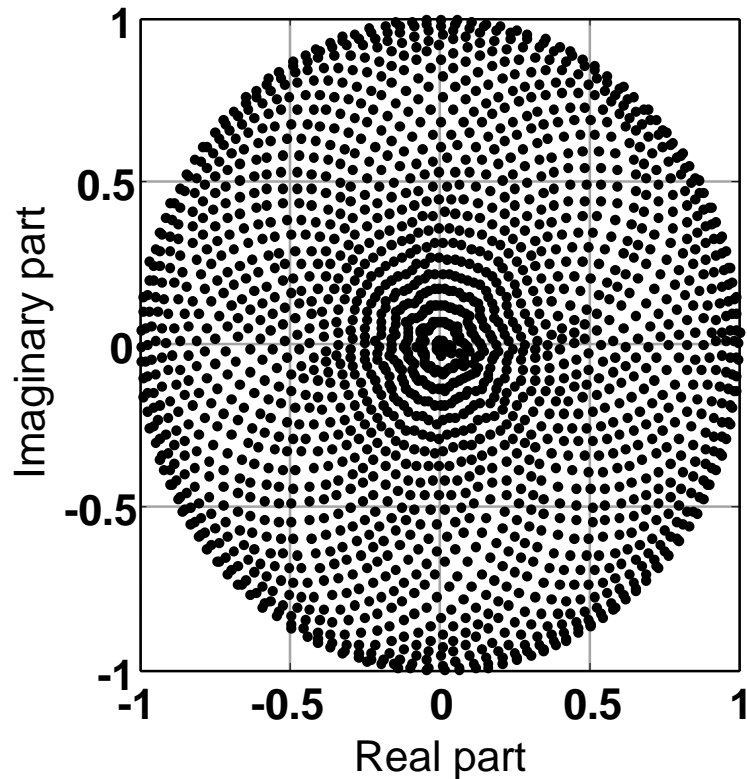


Spannungsversorgungs- und HF-Platine

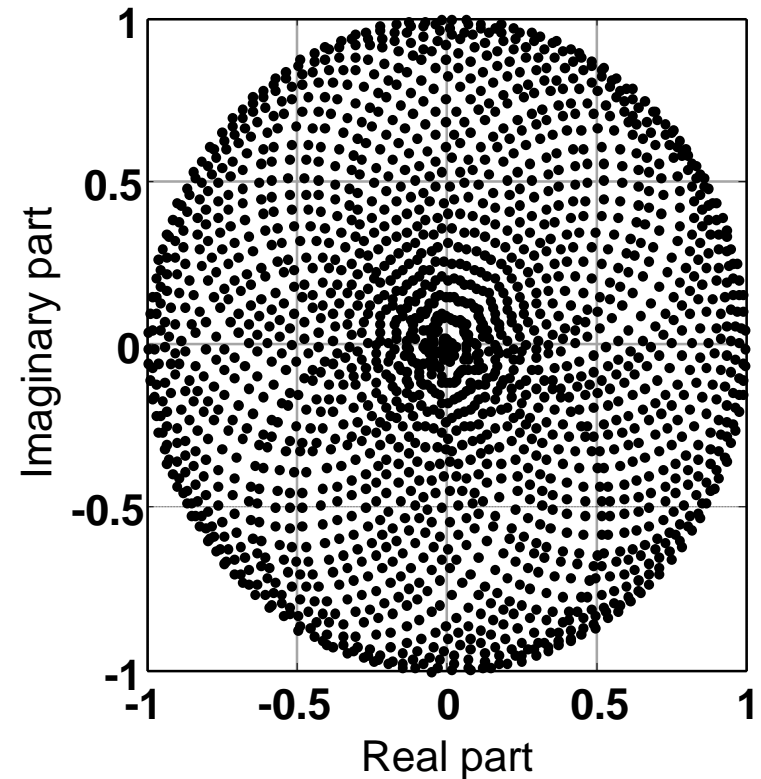


Gemessene statische Konstellationsdiagramme

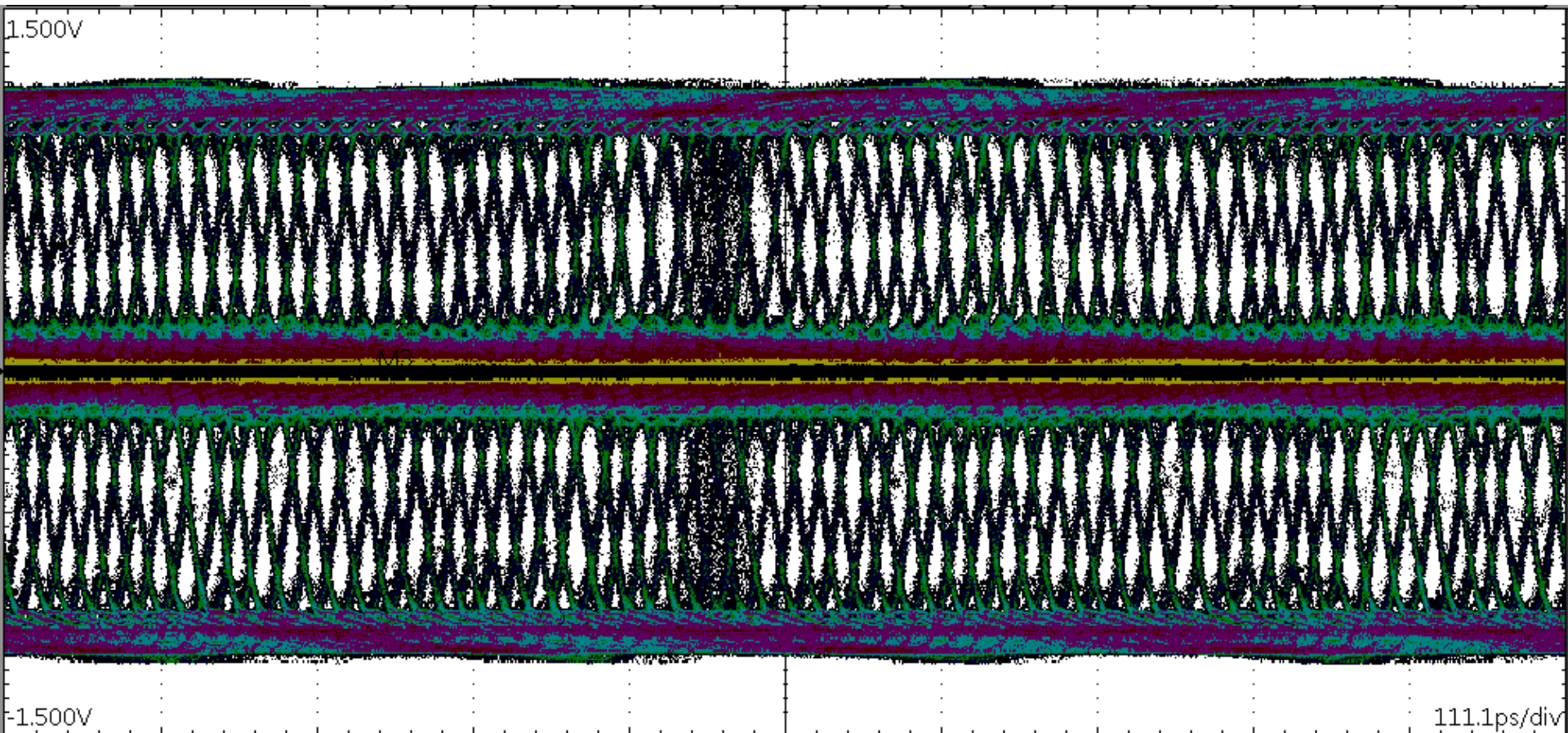
900 MHz



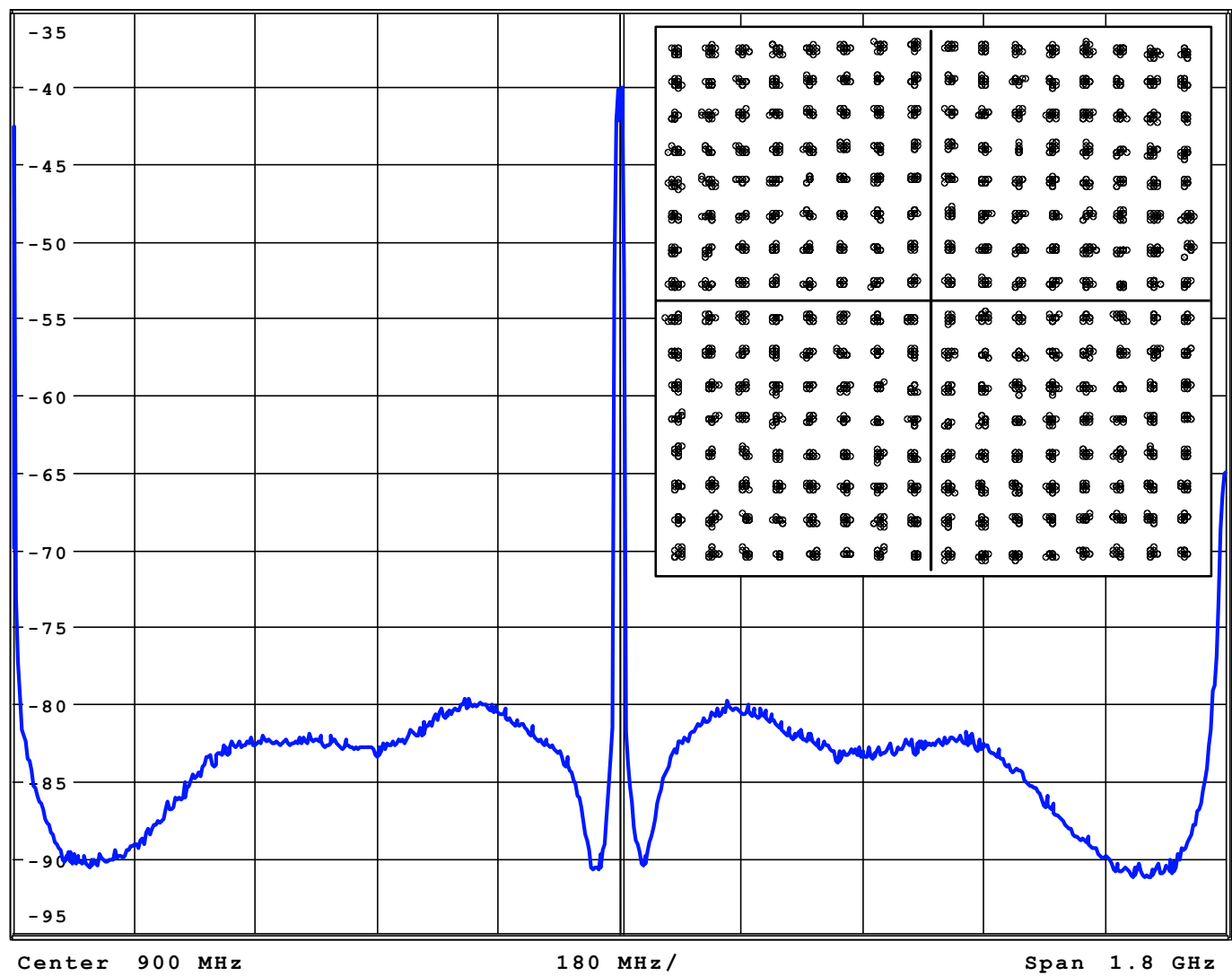
2016 MHz



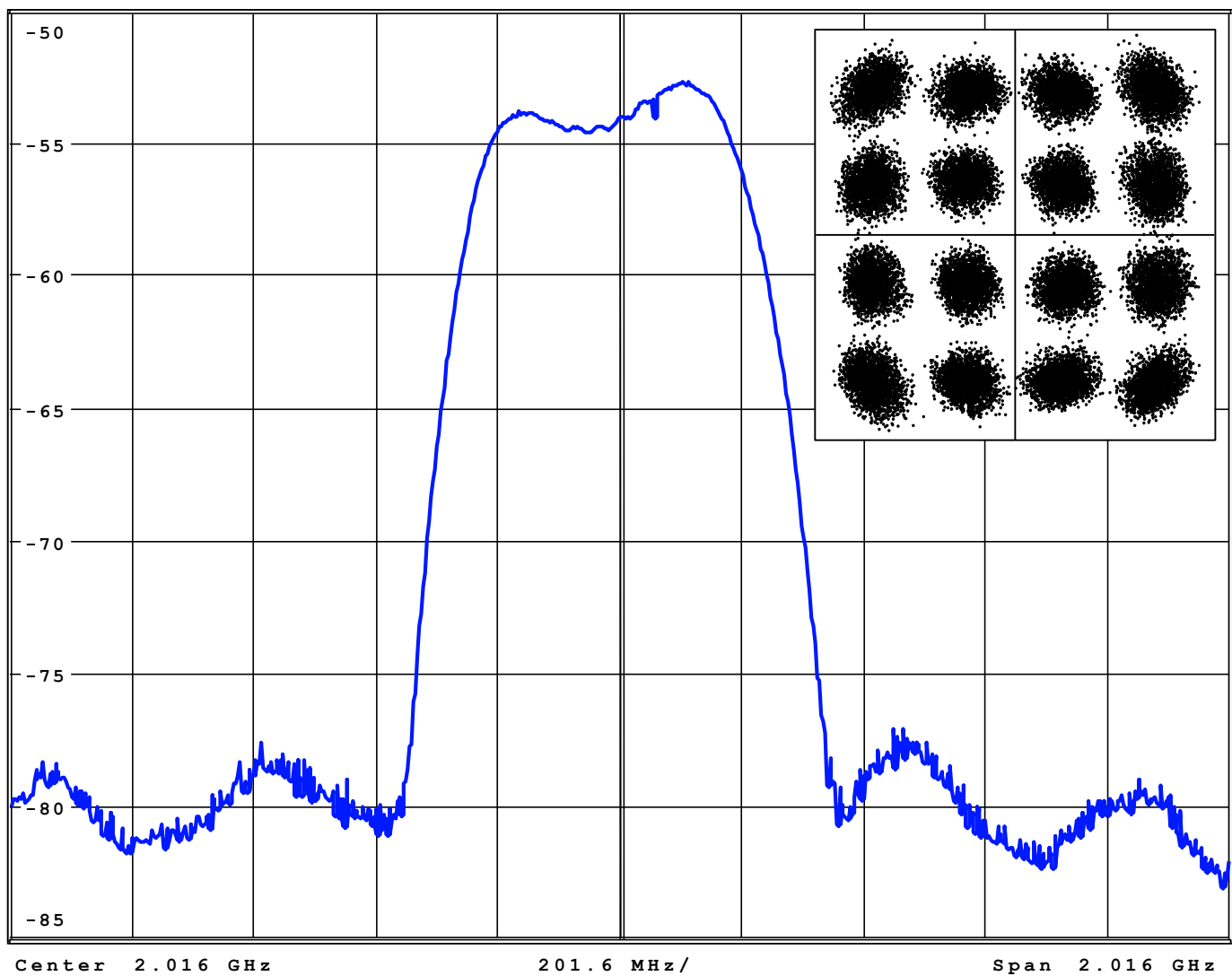
Augendiagramm bipolares Σ -Ausgangssignal bei 900 MHz



900 MHz-HF-Signal moduliert mit 14 MBd QAM-256 (112 Mb/s)



2016 MHz-HF-Signal mod. mit 504 MBd QAM-16 (2016 Mb/s)



ZUSAMMENFASSUNG MESSERGEBNISSE

Property	Unit	1	2	3	4	5
Carrier freq.	MHz	900	2016	2016	2016	2016
Symbol rate	MBd	14.06	15.75	31.50	63.00	504.0
Modulation	QAM	256	256	256	64	16
Data rate	Mb/s	112.5	126.0	252.0	378.0	2016
EVM	%	1.83	2.36	2.47	3.97	13.5
SNDR	dB	34.7	32.5	32.1	28.0	17.4
BER *		$< 10^{-8}$	$1 \cdot 10^{-6}$	$3 \cdot 10^{-6}$	$1 \cdot 10^{-8}$	$1.5 \cdot 10^{-4}$ **
Ch. BW	MHz	18.0	22.5	45.0	90.0	720
Ch. spacing	MHz	20.0	25.0	50.0	100.0	800
BW efficiency	b/Hz	6.22	5.6	5.6	4.2	2.8
ACLR1 _{,Lower}	dB	-44.8	-42.9	-42.2 /	-38.4	-24.7
ACLR1 _{,Upper}	dB	-44.8	-41.8	-40.7	-36.1	-25.1
ACLR2 _{,Lower}	dB	-49.2	-49.0	-45.7 /	-36.1	-20.1
ACLR2 _{,Upper}	dB	-48.6	-47.1	-43.6	-37.3	-23.7

*) estimated [6] **) measured

VERGLEICH MIT DEM STAND DER TECHNIK

Property	Unit	[7]	[8]	[9]	[10]	This Work
CMOS techn.	nm	32	40	45	28	28
carrier frequen. range	GHz	2.4	0.9 - 2.6	1.0 - 3.0	0.35 - 2.6	0.17 - 2.8
max signal BW ¹	MHz	40	40	N/A	400	504
binary outputs		yes	yes	yes	no	yes
carrier freq.	MHz	2400	2000	2400	2000	2016
DC power	mW	82	91	35	670	58
signal type		WLAN	WLAN	GMSK	OFDM	SC RC ²
QAM order		64	64	4	64	256
data rate	Mb/s	54	54	20	120	126
bandwidth	MHz	20	20	N/A	20	22.5
EVM	dB	-32	-29	-33.5	-29	-32.5
PAPR	dB	N/A	8 ³	0	8	6.5
ACLR1	dBc	N/A	-30 ³	N/A	-40	-42

1) demonstr. by experiment 2) single carrier raised cosine with $\beta = 0.5$

3) 20 MHz BW DMT signal

ZUSAMMENFASSUNG

- Technologie: 28 nm FDSOI CMOS (STM)
- Versorgungsspannung: 3x 1.0 V (Digitalteil, Analoge DLL, Ausgang)
- Leistungsaufnahme: 38 mW bei 900 MHz
58 mW bei 2016 MHz
- Verzögerungszelle
 - Voll-Differenziell
 - Gestapelte MOSFETs zur Verzögerungszeit-Kontrolle
 - Grob-Einstellung über Gate-Spannung
 - Fein-Einstellung über Backgate-Spannung
- Integrierender Phasendetektor
 - Neue Topologie
 - Ohne Latch / Gedächtnis
 - Sehr geringe Jitter-Erzeugung
- PPWM-HF-Ausgangssignale mit
 - größter Signalbandbreite (504 MBaud bei QAM-16)
 - höchste Modulationsordnung (QAM-256, bei 14 MBaud)
 - gutes EVM (1,83 %) für Modulation mit veränderlicher Einhüllender/Amplitude (PAPR = 6.5 dB, QAM-256) bei 14 MBaud
- Sauberes Spektrum fern vom Träger
wegen hoher Update-Rate für PW&PC ($f_{\text{Update}} = f_{\text{RF}}$)

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