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32-GS/s SiGe Track-and-Hold Amplifier with 58-GHz Bandwidth and -64-dBc to -29-dBc HD3

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***Abstract*—We demonstrate an ultra-wideband 32-GS/s SiGe track-and-hold amplifier with 58-GHz bandwidth and a compact footprint due to the inductorless design. The circuit achieves a third harmonic distortion of -64 dBc to -29 dBc at 1.0-V_{pp} differential input voltage swing thanks to a linearized switched preamplifier and switched emitter follower stage. It can be especially interesting for direct-conversion 5G mmWave and radar receivers, or systems with a time-interleaving factor of up to 4, as the ultra-high bandwidth spans almost 4 Nyquist bands and covers all designated 5G mmWave frequencies.**

Keywords—analog-digital conversion, analog integrated circuits, bicmos integrated circuits, sampled data circuits, silicon germanium.

I. Introduction

Ultra-wideband receivers are gaining more attention with increasing demand for high data rate and carrier frequency in telecom, defense and instrumentation. Analog front-ends for high performance analog-to-digital converters are one of the main components that need careful implementation, because of their impact on the whole receiver. Concurrent design challenges include high performance specifications for sampling rate, accuracy and bandwidth. Special linearization techniques are necessary to address all of these design goals simultaneously.

Track-and-hold implementations for largest bandwidth are reported in CMOS ([1], [2]), SiGe ([3], [4]), and InP ([5], [6]) as switched capacitor, switched emitter follower or charge-sampling circuits. We use the switched emitter follower topology with a similar linearization technique as in [7]. It mimics the signal path and injects the necessary current to charge the hold capacitance to the voltage sampled by the emitter follower. Therefore, the latter has a constant operating point that does not vary with the input voltage, as it usually would, and results in an increased accuracy at high frequency. In addition, we silence the preamplifier during hold mode, as for instance discussed in [8], among others. This minimizes the unwanted signal feedthrough in hold mode. We add an additional amplifier branch with smaller tail current for subtractive gain composition. Simulations show an increase in bandwidth of 25 % compared with the conventional switched preamplifier and the measured 58-GHz bandwidth at 32 GS/s confirms the benefit of this linearization technique.

Fig. 1 shows the general architecture and a chip micrograph of the sampling circuit. The track-and-hold core comprises a switched preamplifier, a switched emitter follower including hold capacitances and emitter follower buffers. We will explain the utilized linearization techniques in greater detail, first for the switched preamplifier in chapter II and then for the switched emitter follower in chapter III. Experimental results will be presented in chapter IV, and chapter V will conclude the paper.

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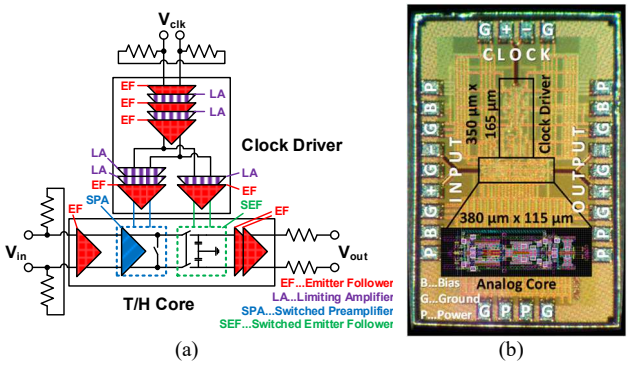
II. Switched Preamplifier

A circuit schematic of the switched preamplifier is shown in Fig. 2. The input transconductance pair Q_{7-8} drives the amplifier branch that is always on and connected to a cascode stage Q_{2-3}. The emitter degeneration resistor $R_{E,0}$ linearizes the operating point of the track-and-hold amplifier (THA) for differential input voltage swings of up to 1 V_{pp}. Higher input voltages are possible, but lead to a degraded linearity. Current sources Q_{10-13} are sized to 20-µm emitter length each to provide low-noise output current for the amplifier branches. They are linearized by resistors R_{0-3} that are designed for a 200-mV voltage drop.

The second input transconductance pair, Q_6 and Q_9, is linearized by $R_{E,1} = R_{E,0}$. Therefore, the gain of both pairs adds up equally to unity gain in track mode, when a positive clock signal switches Q_1 and Q_5 transparent. Collector load resistors $R_C = \frac{R_{E,0}}{3}$ are designed for a maximum differential output voltage swing of 1.5 V_{pp}.

In hold mode, Q_0 and Q_4 conduct the positive signal currents of the switched amplifier branch towards the negative signal currents of the fixed amplifier branch, the same holds for opposite polarity. Both signal currents interfere destructively in both polarities, effectively silencing the differential amplifier output during hold mode. Signal feedthrough to the hold capacitances is strongly attenuated. The additional linearization branch of the switched preamplifier is marked in blue. We apply subtractive gain composition to the transfer characteristic of the amplifier, as illustrated in Fig. 3. The obvious effect is an increase in linear input voltage range with slightly decreased maximum gain. Furthermore, the linearization technique can aid in attenuating the third harmonic distortion. Gain g of the differential amplifier, comprising gains g_1 and g_2 of both branches, can be expressed with a Taylor-series approximation up to the 3rd order as

$$g = g_1 + g_2 = \alpha_1 + 3\alpha_3 v_{in}^2 - \beta_1 - 3\beta_3 v_{in}^2.$$



(a) (b)

Fig. 1. (a) Block diagram of the 32-GS/s track-and-hold amplifier, (b) micrograph of the chip with pad-limited dimensions of 1.5 mm x 1.0 mm.

By stretching the transfer characteristic of both amplifier branches in both directions, by p for gain and q for input voltage v_{in}, the gain characteristic changes to

$$g_{1,p_\alpha,q_\alpha} = p_\alpha g_1(q_\alpha v_{in}) = p_\alpha \alpha_1 + 3p_\alpha \alpha_3 q_\alpha^2 v_{in}^2 \text{ and}$$

$$g_{2,p_\beta,q_\beta} = p_\beta g_2(q_\beta v_{in}) = -p_\beta \beta_1 - 3p_\beta \beta_3 q_\beta^2 v_{in}^2.$$

For $p_\alpha \alpha_1 \gg p_\beta \beta_1$ and $p_\alpha \alpha_3 q_\alpha^2 = p_\beta \beta_3 q_\beta^2$, the third-order term can be neglected without strong attenuation of the fundamental tone and the total gain is simply

$$g = g_{1,p_\alpha,q_\alpha} + g_{2,p_\beta,q_\beta} = p_\alpha \alpha_1 - p_\beta \beta_1.$$

In the circuit, gain variation p is achieved by input transistor size and tail current adjustment through Q_{18-19} and R_{4-5}, whereas a variation in linear input voltage range q is realized by changing the emitter degeneration resistor $R_{E,2}$. This technique proves valuable in increasing the bandwidth of the circuit by 25 % in simulations, whereas dynamic range is improved by 2–3 dB. The additional linearization branch decreases the small-signal gain by -0.9 dB and adds some DC power consumption, although the latter is almost negligible in comparison, as the tail current of the main amplifier is more than 11 times as high.

III. Switched Emitter Follower

Various implementations of ultra-wideband THAs use the switched emitter follower, similar to the one in Fig. 4. The inherent unity gain of the emitter follower transistor Q_0 across a wide frequency range is used to store the input voltage on the hold capacitance C_H during track mode, when Q_4 allows the tail current to pass from Q_5 and R_2 through Q_2 to Q_0. Due to the small base currents, input resistor R_1 has almost no effect in track mode. In hold mode, the tail current is steered towards the other branch, as a low differential clock level switches Q_3 transparent. The tail current continues through Q_1 and R_1 to the load resistors R_C of the preamplifier, causing proportional voltage drop to switch off Q_0. R_1 helps to further decrease the base voltage of Q_0 without leading to an unfavorable operating point in the switched preamplifier, although it slightly decreases the bandwidth. In a differential design, feedforward capacitance C_{FF} can help to avoid unwanted signal feedthrough during hold mode. The base-emitter capacitance $C_{BE,0}$ of Q_0 presents a low-impedance path for input signals at high frequencies. If $C_{FF} = C_{BE,0}$ and connected to opposite polarities of input and output terminals, as depicted in Fig. 4, both positive and negative signals pass through and their destructive interference keeps the output voltage constant. A linearization concept for the switched emitter follower in GS/s-rate sampling circuits is explained in [7]. It consists of two parts – a stabilization mechanism for the sampling emitter follower transistor and a silencing technique during hold mode. As we are using the switched preamplifier for silencing, only a version of the stabilization technique is implemented in the presented switched emitter follower. The linearization branch is, in most regards, a copy of the principal switched emitter follower with Q_{10} as the emitter follower transistor. However, the second hold capacitance C_H is not connected to a fixed supply voltage, but to the emitter node of Q_2 in the track mode branch of the principal switched emitter follower.

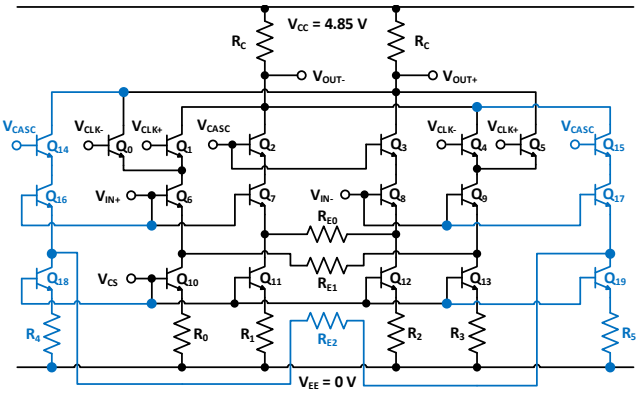


Fig. 2. Circuit schematic of the switched preamplifier with the linearization branch marked in blue.

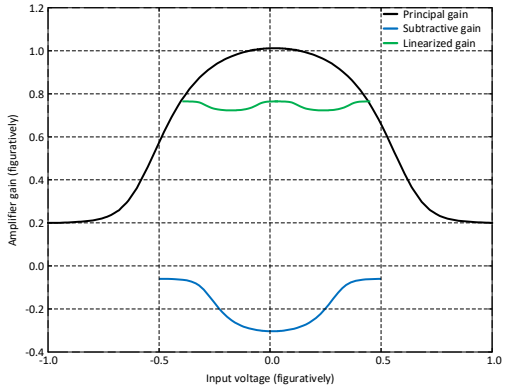


Fig. 3. Linearization by subtractive gain composition in the preamplifier.

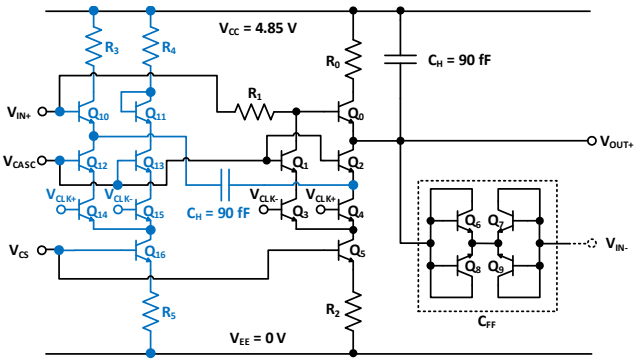


Fig. 4. Circuit schematic of the switched emitter follower with the linearization branch marked in blue. According function in opposite polarity.

This topology injects the charging current i_{C_H} of C_H into the emitter of Q_2 that is needed for the output voltage of the principal hold capacitance. It is $i_{E,2} = I_{CS} + i_{C_H}$ and for $\beta \gg 1$, $i_{C,2} \approx i_{E,2}$. This collector current of Q_2 is then separated above into $i_{E,0} = I_{CS}$ and i_{C_H}, which is charging the hold capacitance. The emitter follower transistor Q_0 is no longer driving the charging current for C_H and maintains a constant operating point. This is important because its base-emitter voltage depends on the emitter current and is slightly distorted by i_{C_H} without the linearization branch. A distorted base-emitter voltage $v_{BE,0}$ would result in a distorted output voltage v_{out}, as the emitter follower output follows its base voltage, i.e. $v_{out} = v_{B,0} - v_{BE,0}$. Simulations show an improved dynamic range by up to 12 dB for high frequencies.

The large output driver of the THA could discharge the hold capacitance substantially. Therefore, we inserted an intermediate emitter follower buffer with small tail current to decouple C_H from the output driver. The output buffer achieves differential 100-Ω matching by series resistors, limiting the output amplitude at -6 dB below the input level. For input matching, we use emitter follower input buffers with shunt resistors, both for input and clock terminals, as shown in Fig. 1. A detailed circuit schematic of the clock driver is given in Fig. 5. It is designed to process 1-V_{pp} input voltage swings like the analog core, as high amplitudes at the clock input result in fast switching and low jitter. The clock driver consists of alternating arrangements of emitter follower buffers and differential limiting amplifiers. After the third emitter follower stage, the paths of the switched emitter follower and the switched preamplifier clock separate, as the delay element for the latter needs to be included here. It is designed for an approximate delay of 3 ps, to switch off the switched emitter follower before silencing the preamplifier. Otherwise, the output voltage would be affected and silenced, too. The simple topology and the high sampling rate require large buffers at the output of the clock driver. The additional linearization branch in the switched emitter follower doubles the capacitance at its clock interface, sacrificing power consumption for dynamic range.

IV. Experimental Results

The IC was measured with 40-GHz GSGSG on-wafer probe heads at the input and output side and 20-GHz GSSG probe heads for the clock input and supply voltage, as marked in the chip micrograph in Fig. 1. DC blocks were used at the RF probes to decouple the DC operating points of the IC and measurement instruments. Broadband baluns were used to convert single-ended signals into differential signals at the clock and input probes, where the signal generators were calibrated for a 1-V_{pp} sinewave. Another signal generator was locked by the 10-MHz reference with them to provide a 1-GHz trigger signal for the subsampling oscilloscope. The bandwidth of the differential sampling module is 70 GHz.

Fig. 6 shows the captured single-ended and differential signals for a 15-GHz, 1-V_{pp} input signal in time-domain (a) and in frequency-domain (b). A 256-point DFT with one point per hold interval was applied to the transient signal to calculate the frequency spectrum, as depicted with white diamonds. The RMS noise voltage is 3.5 mV with deembedded oscilloscope noise and includes white noise and sampling jitter. It is determined as the standard deviation of 512 samples at 32 GS/s and 32 GHz, where every sample has the same expected value. It still contains noise induced by synchronization errors between clock and signal generator.

Fig. 6 (c) shows the large-signal frequency response of the circuit with 58-GHz bandwidth, where the output amplitude is -3 dB below the value at 2 GHz. The gain is normalized to the maximum output voltage of the resistive voltage divider, as mentioned in section III. For the calculation of harmonic distortion, the transient signal of 512 hold phases with 64 averages is transformed into frequency domain. The decreased noise bin voltage helps to visualize harmonics, especially for high signal frequencies. Fig. 6 (d) shows the calculated harmonic distortion with corresponding accuracy thresholds. Total harmonic distortion (THD) is dominated by the third harmonic distortion (HD3) in most of the first Nyquist band and by the second harmonic distortion of the signal generator above. HD3 corresponds to 6-bit accuracy in the first Nyquist band, 5-bit accuracy in the second and third Nyquist band, and stays at min. 4-bit accuracy up to 61 GHz. Global minima and maxima are -64 dBc at 46 GHz and -29 dBc at 57 GHz. THD stays within -41 dB and -14 dB, respectively. SNR calculated from the gain and RMS noise voltage accounts to 27–34 dB.

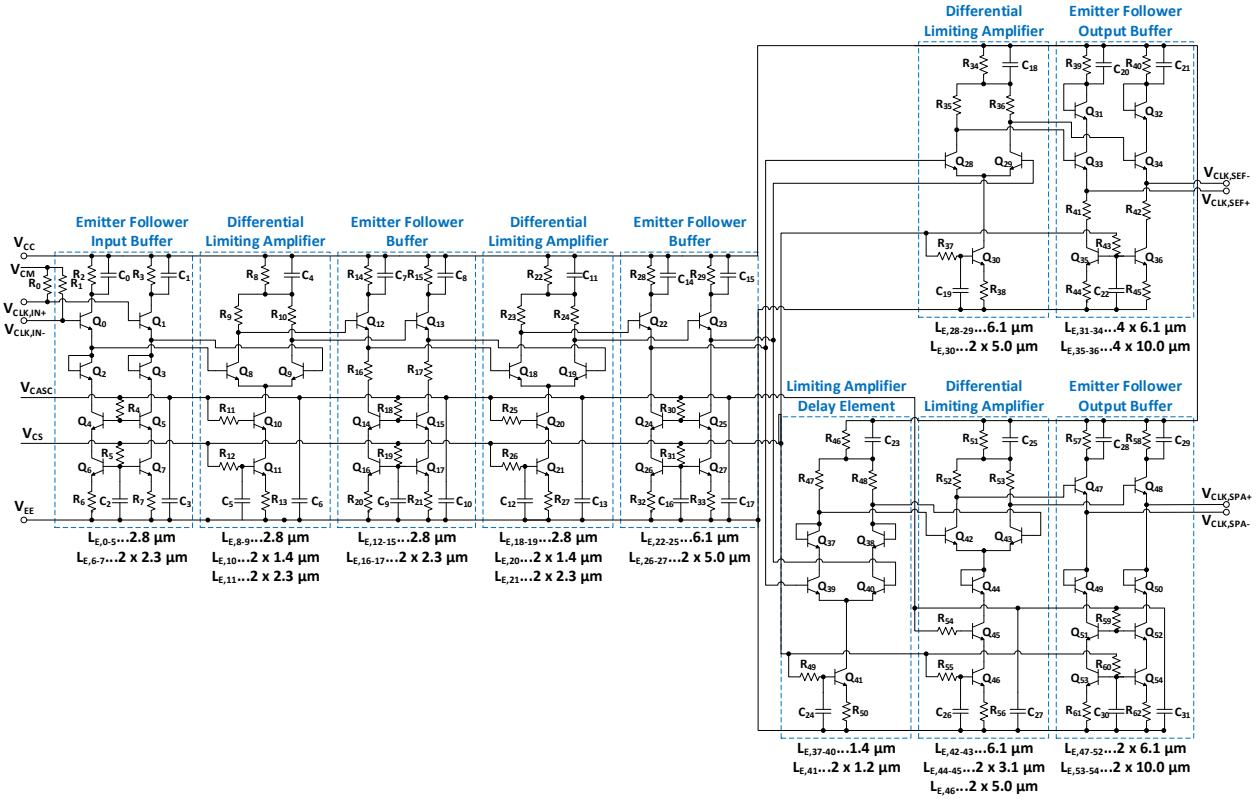
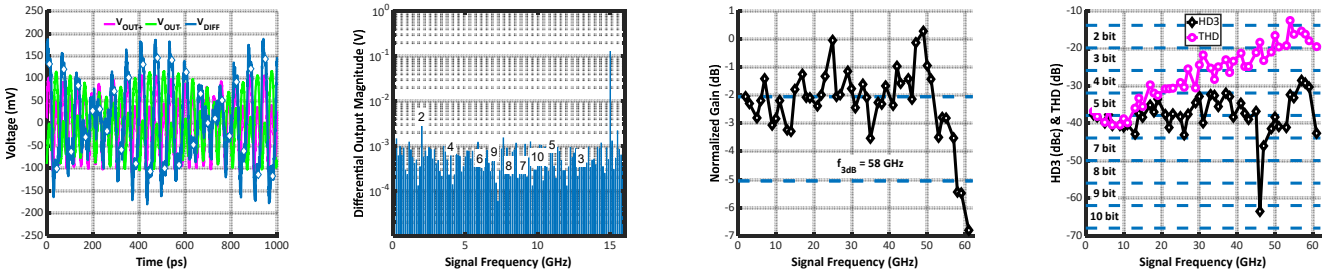


Fig. 5. Clock driver for the switched preamplifier (SPA) and the switched emitter follower (SEF) of the track-and-hold amplifier, based on limiting gain stages, emitter follower buffers and a delay element for optimized timing between SPA and SEF clock. Emitter lengths L_E are given for each stage.



(a) (b) (c) (d)

Fig. 6. Measurement results of the 32-GS/s track-and-hold amplifier with 1-V_{pp} input voltage swing. (a) Transient output signal and (b) frequency spectrum of 256 hold phases at 15-GHz, (c) large-signal frequency response, and (d) harmonic distortion of 512 hold phases with 64 averages up to 61 GHz.

Table I summarizes published state-of-the-art performance figures. Our described linearization techniques enable the highest THA bandwidth without inductors to date. The 70-GHz bandwidth of the THA documented in [4] is the highest overall, followed by the presented 32-GS/s THA with 58 GHz and the CMOS circuits in [1] and [2] with 55 GHz. The circuit presented in this work achieves similar HD3, although especially the CMOS implementation in [1] consumes significantly less power. However, this circuit is the only ultra-wideband THA measured at 1.0-V_{pp} input voltage swing. Therefore, significantly better results can be expected for smaller input voltage swings. Among the circuits where technology parameters were given, the presented THA is realized with lowest transistor transit frequency like the one in [3], but accomplishing faster sampling rate and higher bandwidth at a larger input voltage swing.

V. Conclusion

We demonstrate a 32-GS/s THA with improved bandwidth and accuracy. Employing subtractive gain composition in the switched preamplifier yields a 25 % bandwidth improvement. A linearized operating point of the switched emitter follower allows an increase in accuracy by up to 12 dB for high frequencies. The measured performance of 58-GHz bandwidth and -64-dBc to -29-dBc HD3 allow for an application in a 32-GS/s 6–8-bit single-core ADC e.g. for direct-conversion 5G mmWave and radar receivers, or in ultra-high data rate 4-fold time-interleaving systems with 128 GS/s, like data center interconnects or instrumentation.

Acknowledgment

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TABLE I. Comparison of Ultra-Wideband Track-and-Hold Amplifiers

Reference	Sampling Rate	Bandwidth	Input Voltage Swing	Third Harmonic Distortion	Total / Core Power Consumption	Technology f_T / f_{max}
[1]	25 GS/s	55 GHz	0.8 V_{pp}	-35 dBc to -23 dBc (3–67 GHz)	0.07 W / –	28 nm CMOS – / –
[2]	4 x 8 x 4 GS/s = 128 GS/s	55 GHz	0.5 V_{pp}	-30 dBc (1 GHz & 22 GHz)	0.3 W / 120 mW	22 nm CMOS – / –
[3]	25.6 GS/s	40 GHz (1-dB BW)	0.5 V_{pp}	-44 dBc to -32 dBc (1–25 GHz)	0.9 W / 123 mW	130 nm SiGe 250 / 400 GHz
[4]	40 GS/s	70 GHz	0.45 V_{pp}	-48 dBc to -32 dBc (1–19 GHz)	– / 440 mW	130 nm SiGe 300 / 500 GHz
[5]	50 GS/s	50 GHz	0.4 V_{pp}	-62 dBc to -46 dBc (0–17 GHz in track mode)	1.9 W / –	700 nm InP 320 / – GHz
[6]	70 GS/s / 60 GS/s	51 GHz	0.4 V_{pp}	-52 dBc to -37 dBc (0–15 GHz)	1.9 W / –	700 nm InP 320 / – GHz
This Work	**32 GS/s**	**58 GHz**	**1.0 V_{pp}**	**-64 dBc to -29 dBc (2–61 GHz)**	**1.8 W / 685 mW**	**130 nm SiGe 250 / 400 GHz**