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WFC - Enabling technologies for efficient ultra-high speed wireless communication systems towards 100 Gb/s at

2021 IEEE International Microwave Symposium Virtual Event (IMS), Altanta, GA, USA
June 20-25, 2021.

WFC-8

High-Bandwidth Analog-to-Digital-Converter Front-Ends in SiGe-BiCMOS Technology

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Institute of Electrical and Optical
Communications Engineering

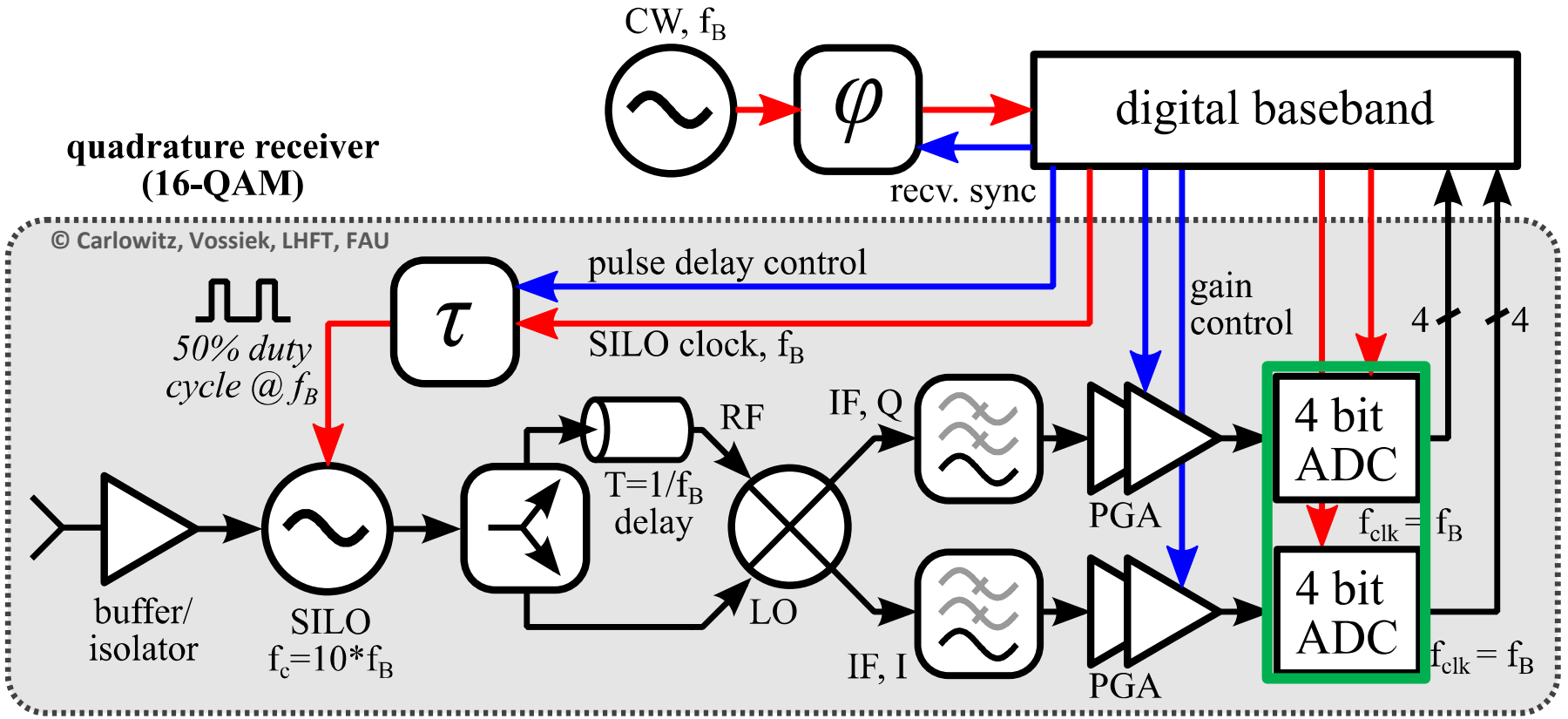
Outline

- Introduction
  - Motivation: Broadband Wireless & Optical Data Links
  - ADC Interleaving Methods: STI, ATI, FDI
  - ADC Signal Processing Chain
- 40 GS/s Track&Hold-less Front-End for 4 bit ADC
- 64 GS/s Voltage Mode Track&Hold Circuit
- Voltage Mode versus Current / Charge Mode Sampling
- 25 GS/s Current Mode Track&Hold Circuit
- 112 GS/s & 128 GS/s Current Mode Analog Demultiplexer Circuits
  - 112 GS/s 1:4 ADeMUX & Application
  - 128 GS/s 1:4 ADeMUX
- Conclusion

High-Bandwidth
Analog-to-Digital-Converter Front-Ends
in SiGe-BiCMOS Technology

INTRODUCTION

Motivation: Wireless Data Links



100 Gb/s =

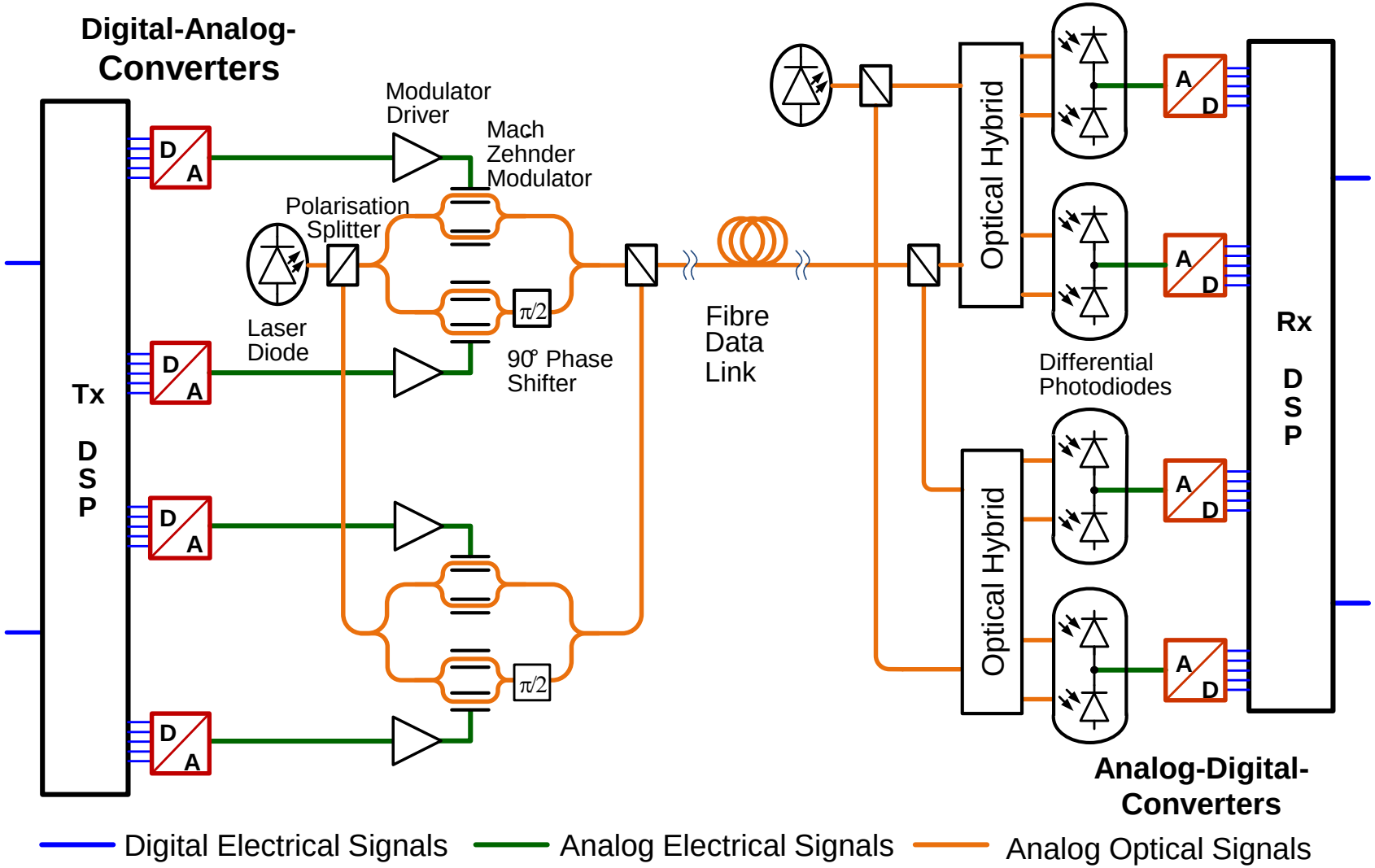
25 GBd x 4 bit/Symbol

25 GBd with 16QAM

f_{RF}	f_{IF}	f_{Baud}	f_S
250 GHz	0 Hz	25 GBaud	25 GS/s

C. Carlowitz, M. Vossiek, "Concept for a novel low-complexity QAM transceiver architecture suitable for operation close to transition frequency," *2015 IEEE MTT-S Int. Microwave Symp.*, 2015, DOI: 10.1109/MWSYM.2015.7166983

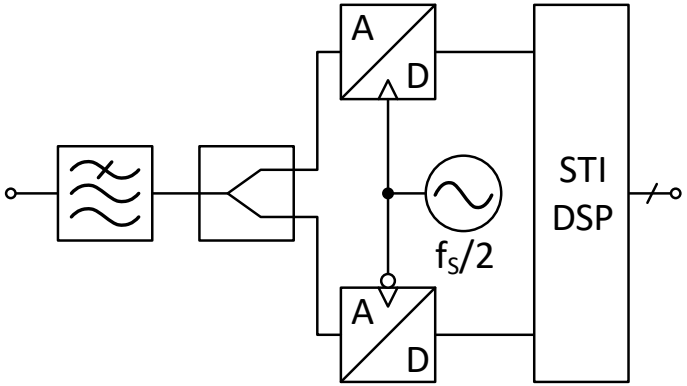
Motivation: Optical Data Links



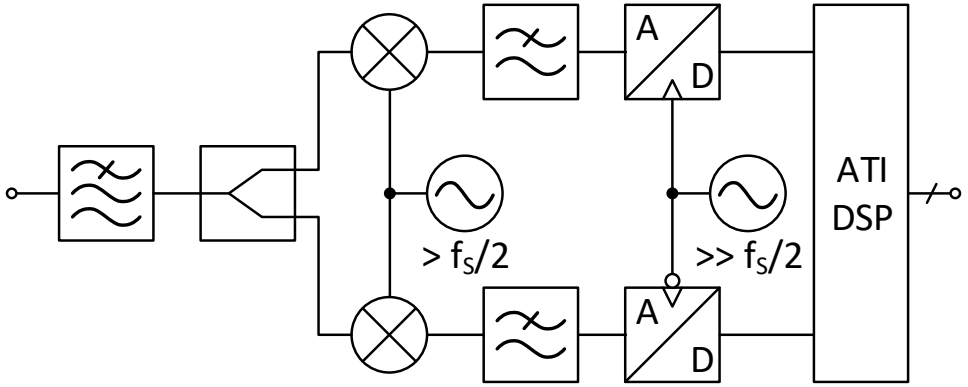
M. Grözing: Manuscript, University of Stuttgart, 2020

ADC Interleaving Methods

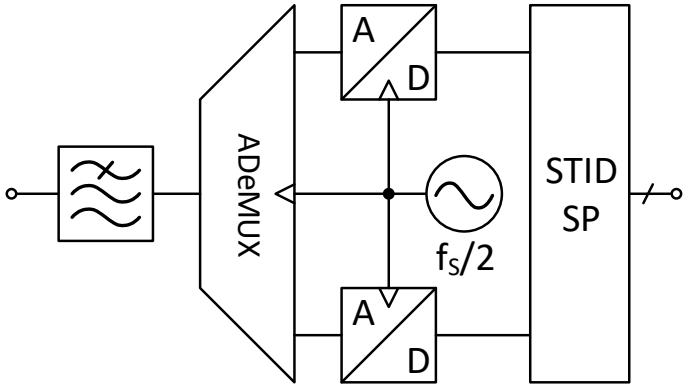
STI
Power-
Adder / Divider



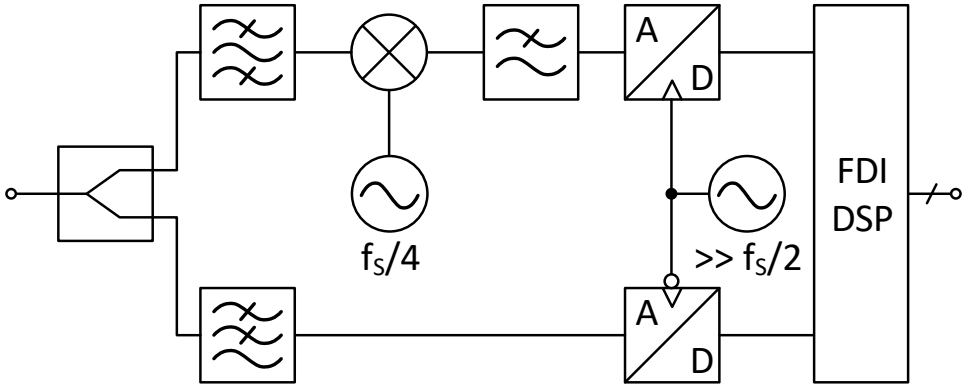
ATI
Up- / Down-
Converters + Filters



STI
Analog Active
MUX / DeMUX

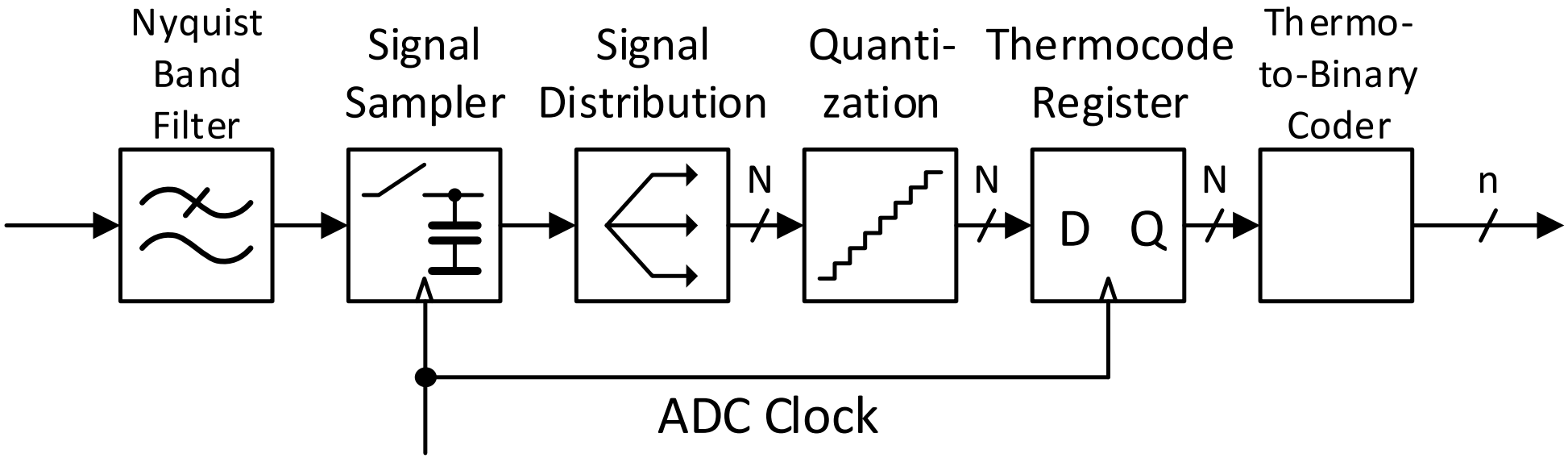


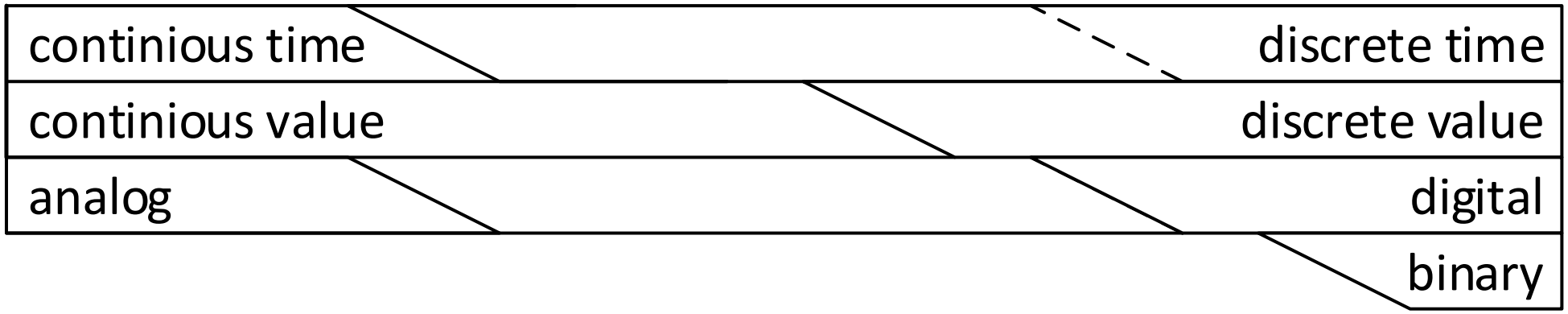
FDI
Up- / Down-
Converters + Filters



M. Grözing: Internal manuscript, 2021

ADC Signal Processing Chain



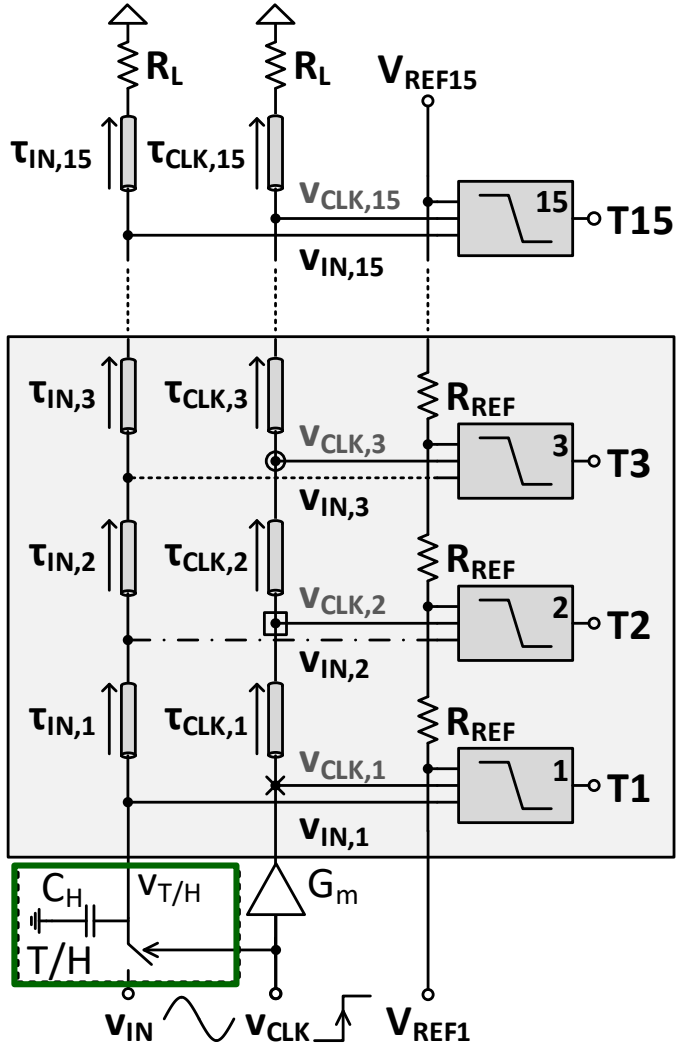


M. Grözing: Internal manuscript, 2021

High-Bandwidth
Analog-to-Digital-Converter Front-Ends
in SiGe-BiCMOS Technology

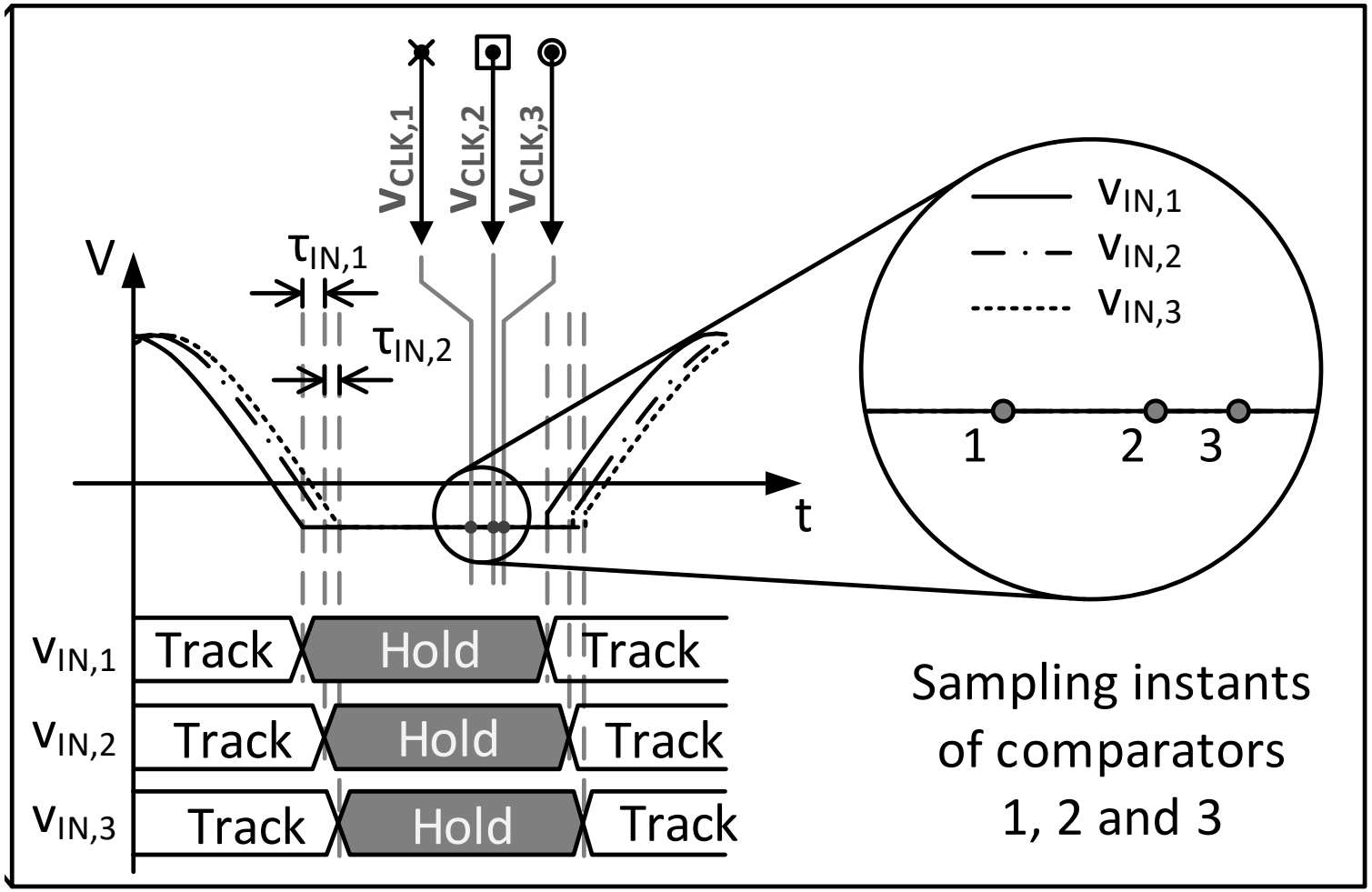
40 GS/s Track&Hold-less Front-End for a 4 bit ADC in 130 nm BiCMOS

40 GS/s Track&Hold-less Front-End (1)



T/H

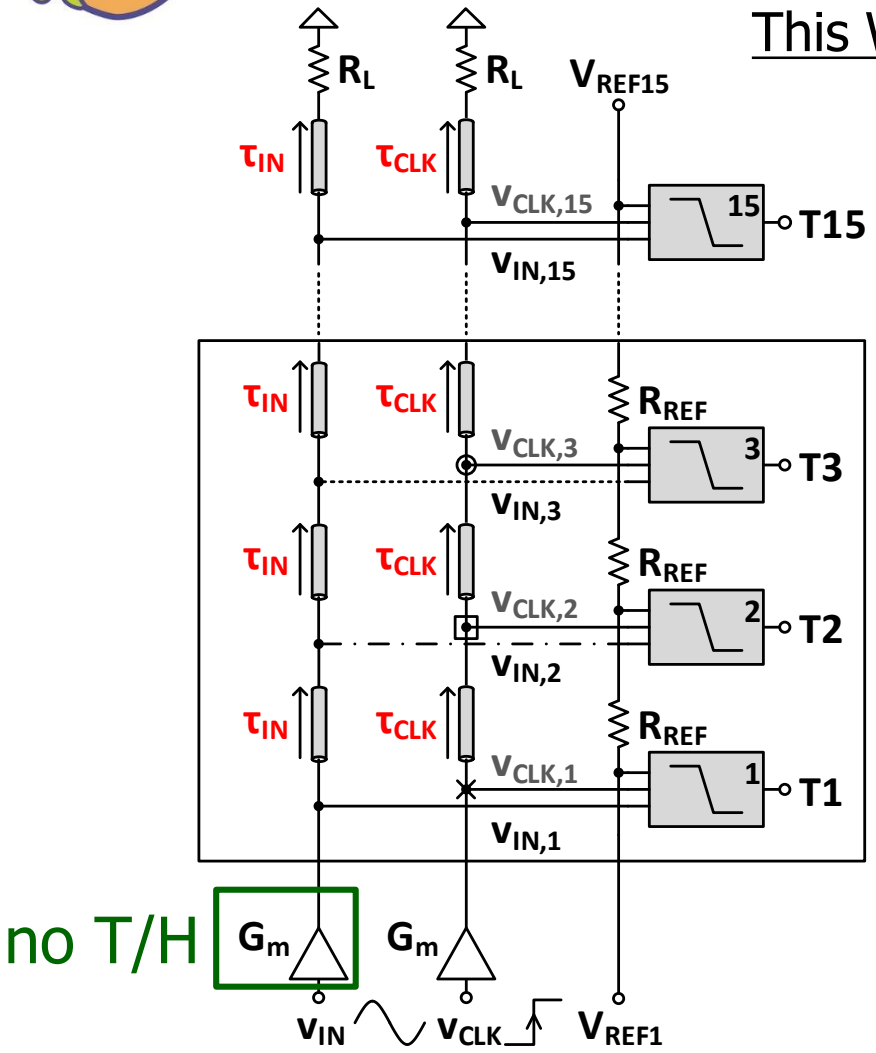
Conventional: with T&H Circuit

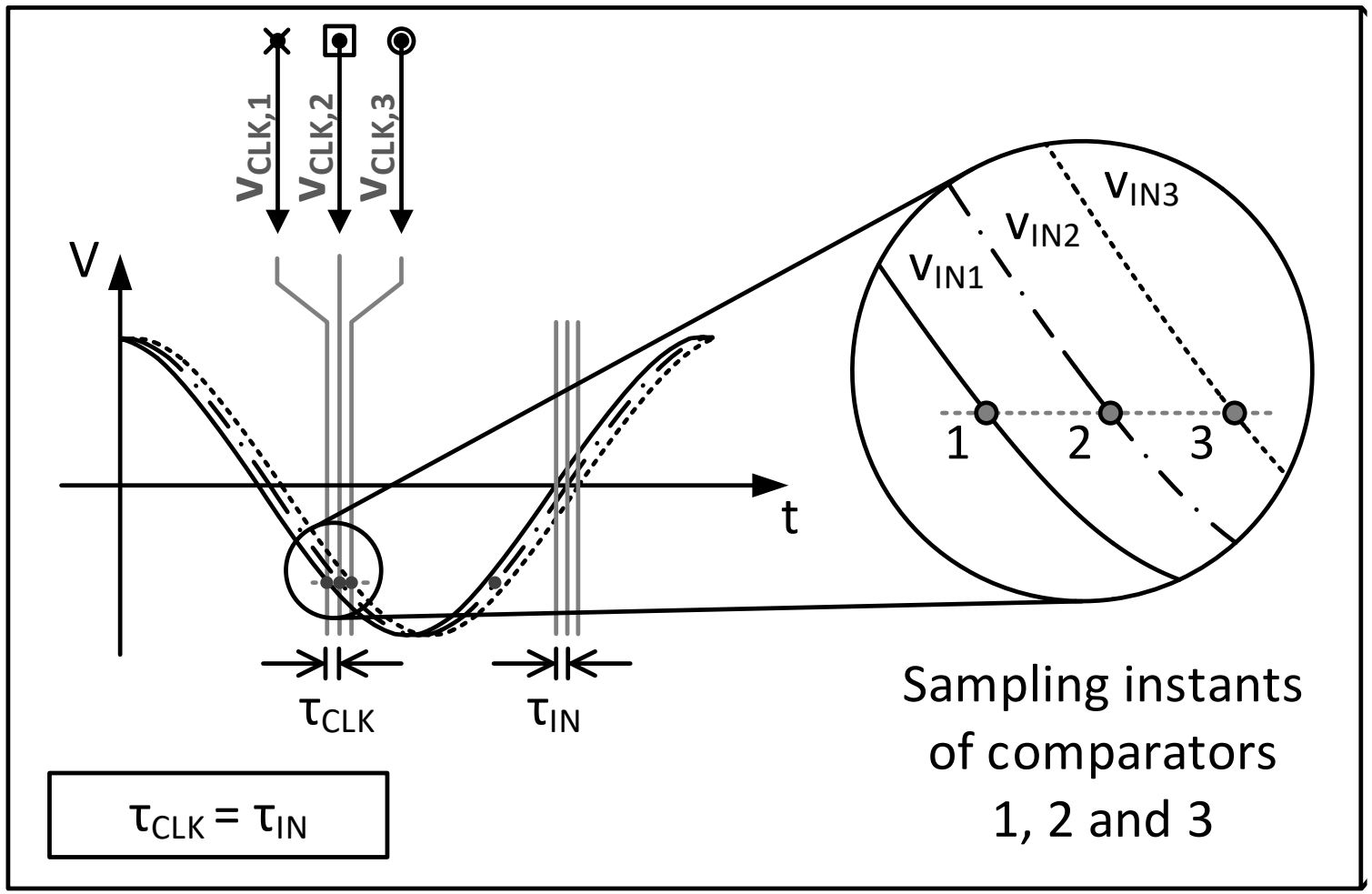


X.-Q. Du, M. Grözing, M. Buck, M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *BCTM 2017*. https://doi.org/10.1109/BCTM.2017.8112929

40 GS/s Track&Hold-less Front-End (1)

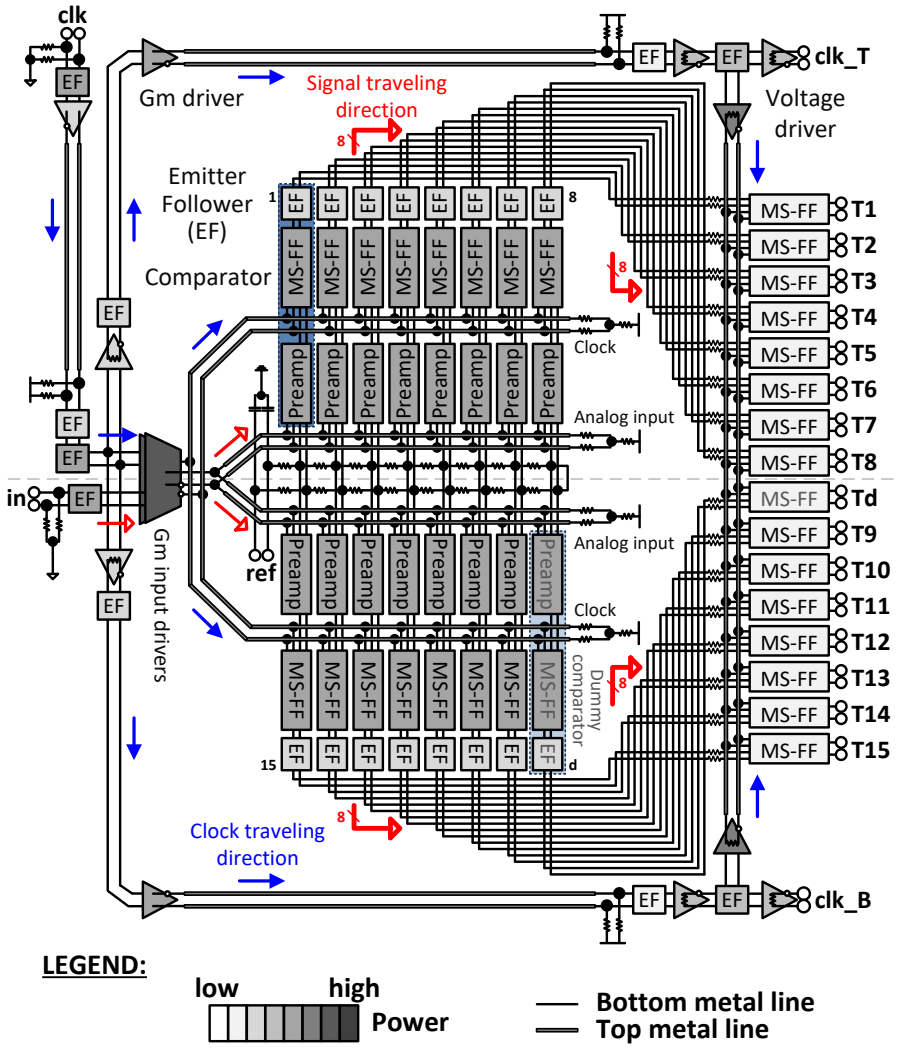
This Work: w/o T&H, matched Transmission Lines for Signal & Clock

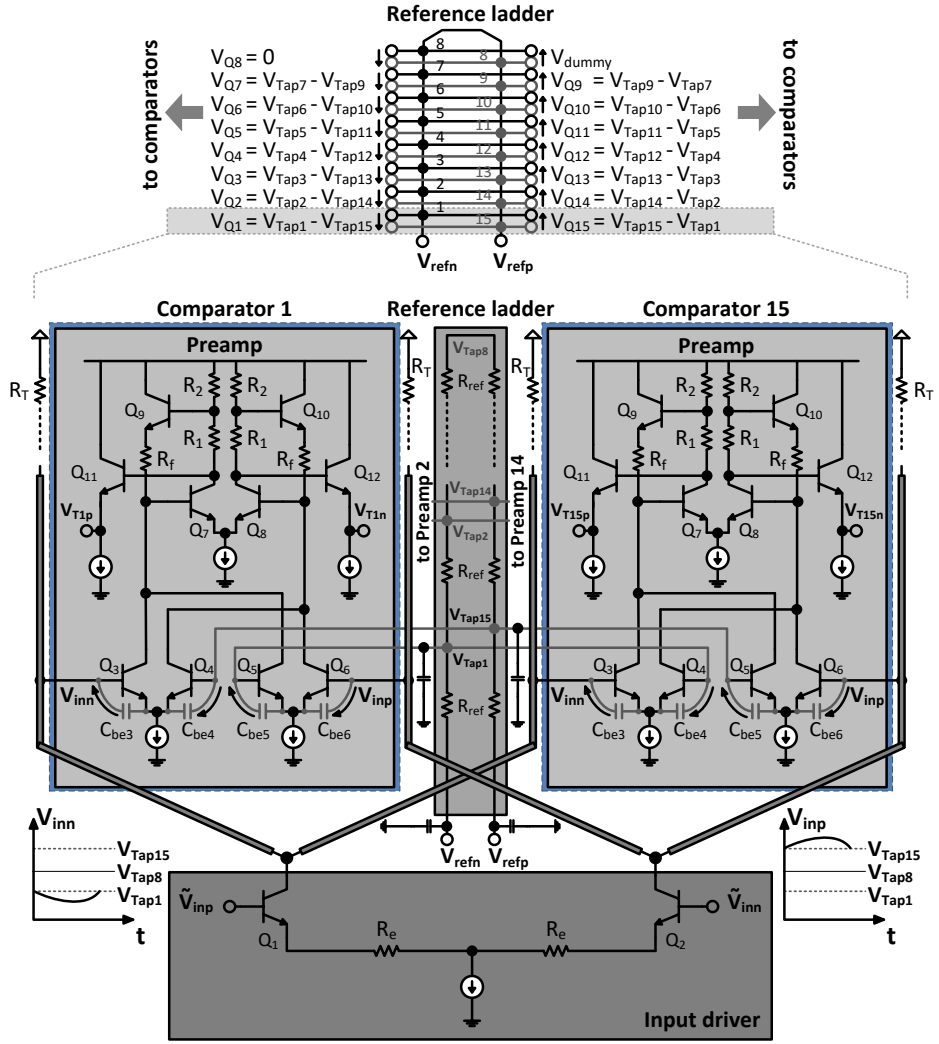




X.-Q. Du, M. Grözing, M. Buck, M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *BCTM 2017*. https://doi.org/10.1109/BCTM.2017.8112929

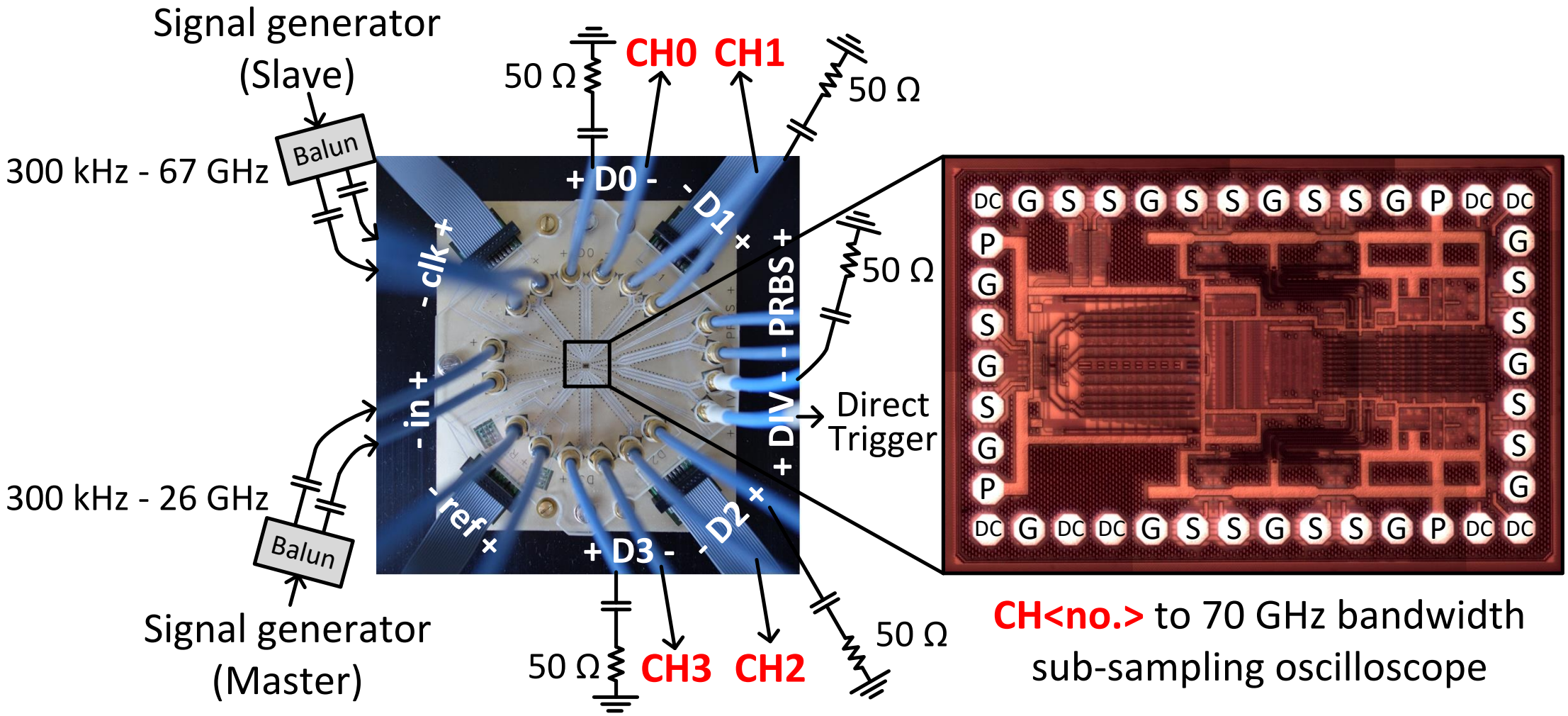
40 GS/s Track&Hold-less Front-End (2)





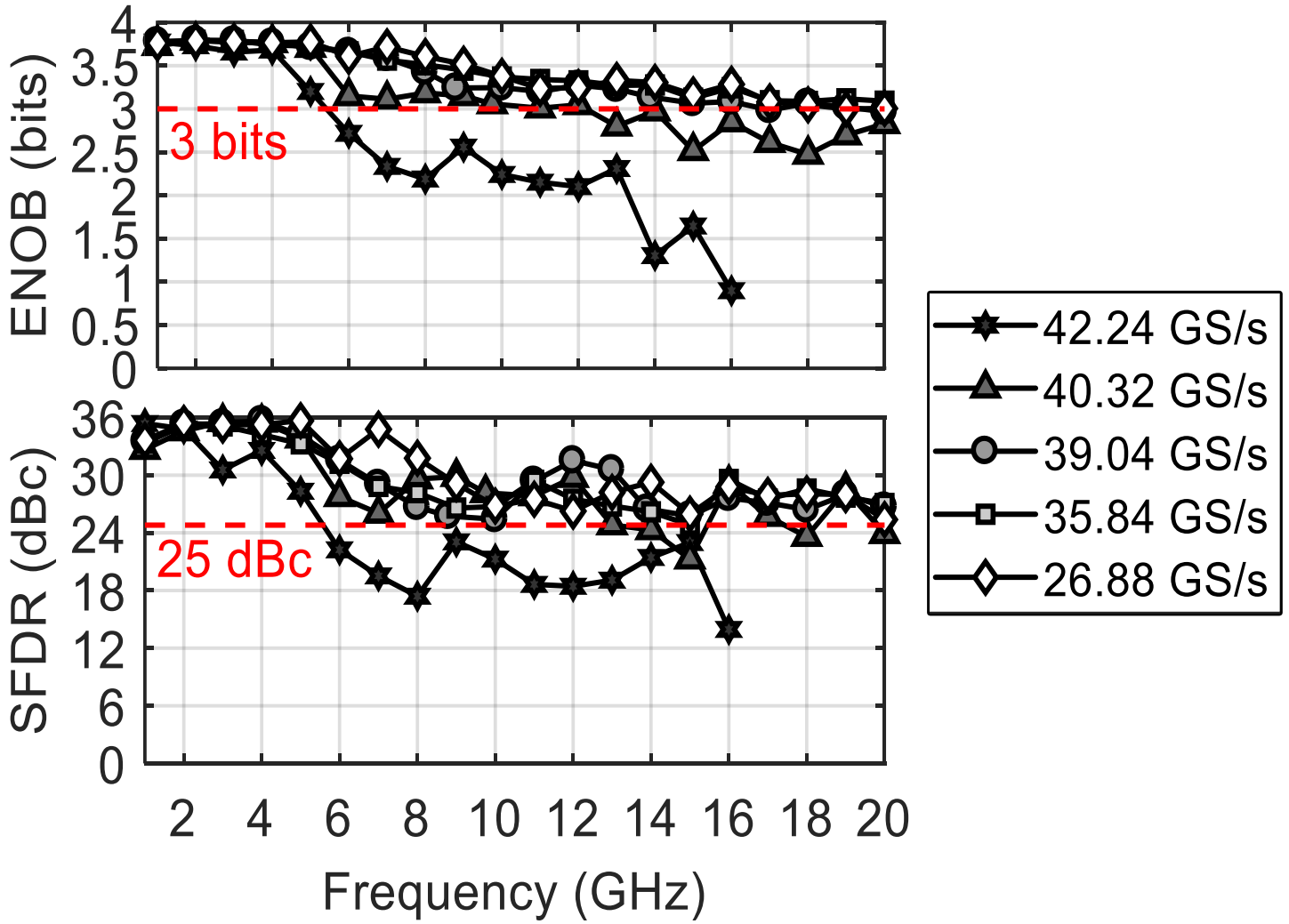
X.-Q. Du, M. Grözing, M. Buck, M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *BCTM 2017*. https://doi.org/10.1109/BCTM.2017.8112929

40 GS/s ADC: Measurement Setup



X.-Q. Du, M. Grözing, M. Buck, M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *BCTM 2017*. https://doi.org/10.1109/BCTM.2017.8112929

40 GS/s ADC: Measurement Results



- ERBW = 16 GHz at 35.84 GS/s
- ENOB ≥ 3 bits from DC to 20 GHz up to 39.04 GS/s
- ENOB ≥ 3 bits from DC to 11 GHz at 40 GS/s

X.-Q. Du, M. Grözing, M. Buck, M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *BCTM 2017*. https://doi.org/10.1109/BCTM.2017.8112929

40 GS/s TH-less ADC: Comparison (2017)

	This work		U of T [2]	TelASIC [3]	Alcatel [4]
Resolution (bits)	**4**		4	3	5
Time-interleaved	**No**		No	No	Yes, 2x
Digital encoder	**Yes**		No	No	Yes
f_{Sample} (GHz)	**35.84**	**40.32**	35	40	50
ENOB (bits)/ f_{in} (GHz)	**3.7/1** **3.1/18**	**3.7/1** **2.8/20**	3.7/1 1.6/15	2.8/0.05 ~1.2/19	4.1/2 3.4/22
ERBW (GHz)	**16**	**8**	8	N/A	18
FOM (pJ/cs)	**8.4**	**8.3**	25.6	33.9	11.6
Die area (mm^2)	**1.4**		8.0	4.0	10.2

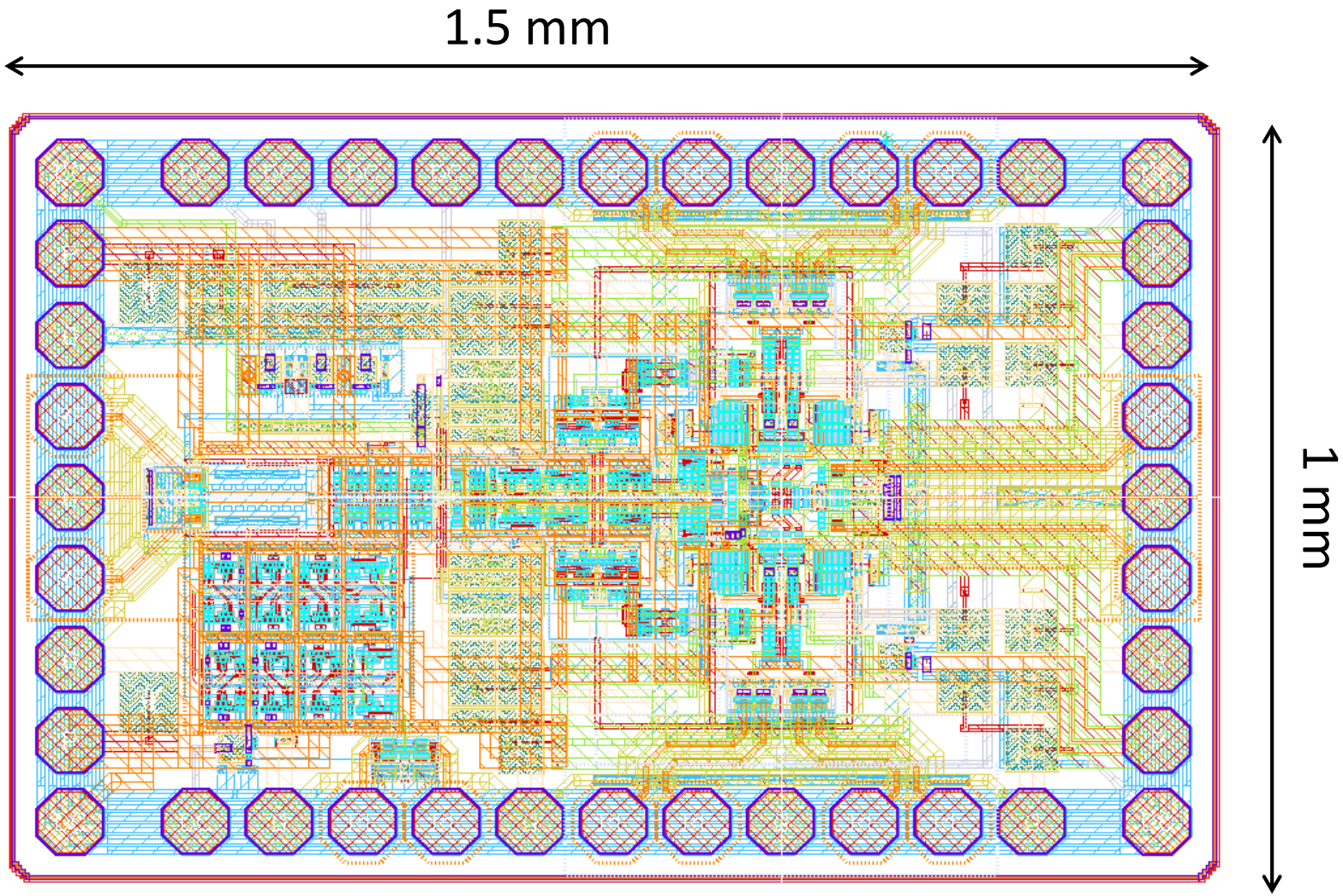
[1] C. Carlowitz and M. Vossiek, "Concept for a novel low-complexity QAM transceiver architecture suitable for operation close to transition frequency," *IEEE MTT-S IMS*, 2015, pp. 1-4.
[2] S. Shahramian, S. P. Voinigescu and A. C. Carusone, "A 35 GS/s, 4-Bit Flash ADC with Active Data and Clock Distribution Trees", *IEEE JSSC*, vol. 44, no. 6, pp.1709-1720, June 2009.
[3] W. Cheng *et al.*, "A 3 b 40 GS/s ADC–DAC in 0.12 µm SiGe", *IEEE ISSCC*, 2004, pp. 262-263.
[4] J. Lee and Y. Chen, "A 50-GS/s 5-b ADC in 0.18-um SiGe BiCMOS", *IEEE MTT-S IMS*, 2010, pp. 900-903.

X.-Q. Du, M. Grözing, M. Buck, M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *BCTM 2017*. https://doi.org/10.1109/BCTM.2017.8112929

40 GS/s TH-less ADC : Summary

- Fastest single-core ADC with digital encoder w/o front-end T&H up to 42 GS/s (2017)

- ENOB ≥ 3 bits from DC-20 GHz up to 39 GS/s



X.-Q. Du, M. Grözing, M. Buck, M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *BCTM 2017*. https://doi.org/10.1109/BCTM.2017.8112929

High-Bandwidth
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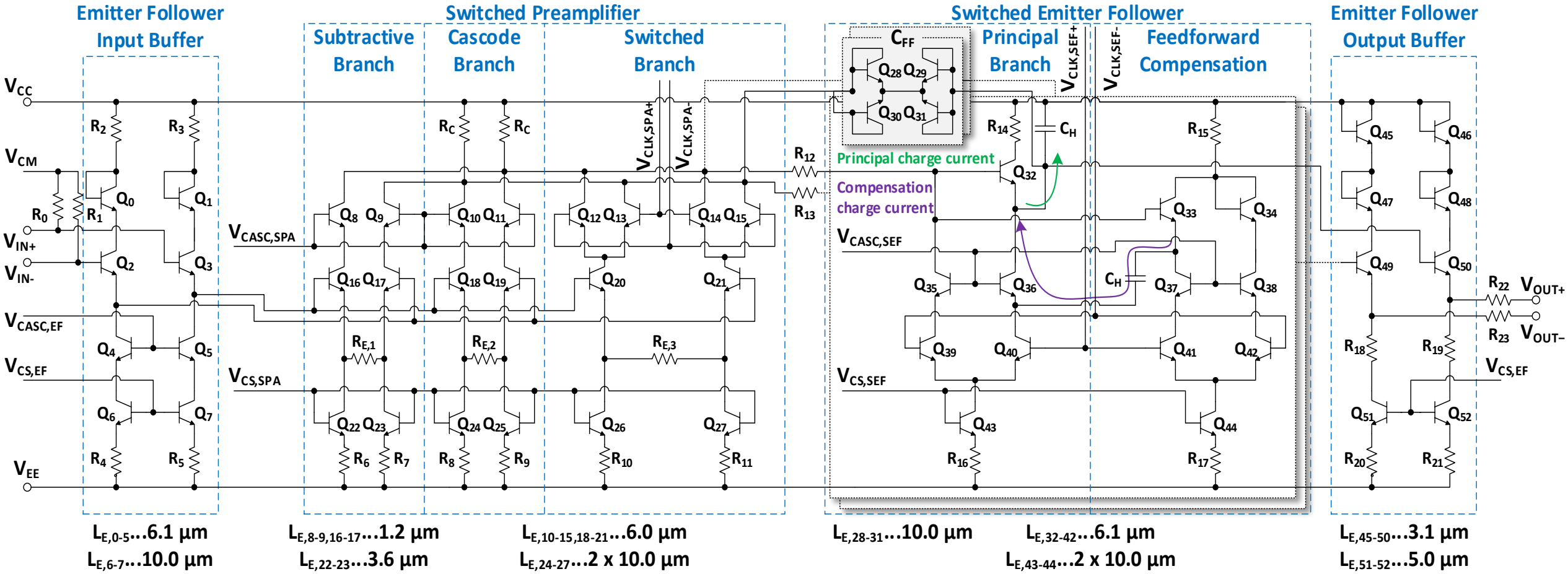
in SiGe-BiCMOS Technology

64 GS/s >61-GHz-3dB-Bandwidth Voltage Mode Track&Hold Circuit

64 GS/s Voltage Mode Sampler (1)

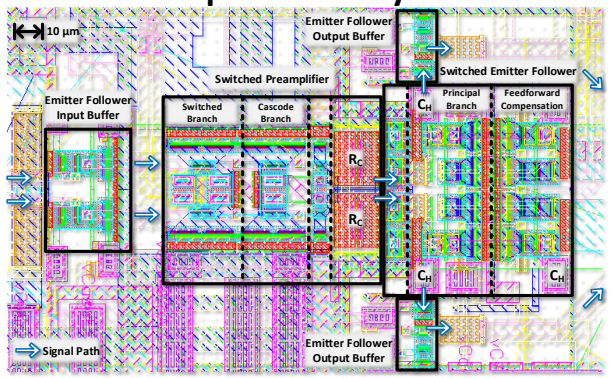
VM-TH Signal Path Schematic



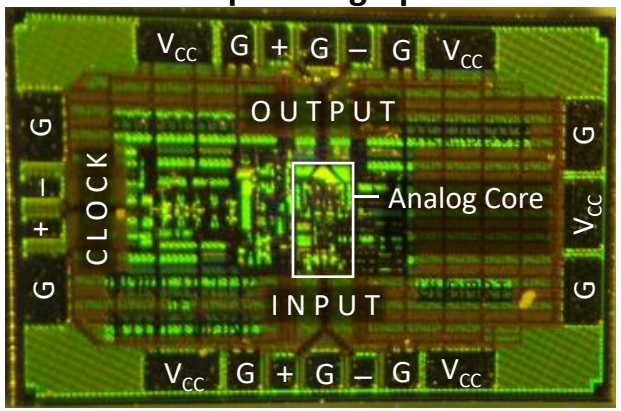
P. Thomas, M. Grözing, and M. Berroth, "64-GS/s 6-bit Track-and-Hold Circuit with More Than 61 GHz Bandwidth at 1.0 V pp Input Voltage Swing in 90-nm SiGe BiCMOS Technology," *ISCAS 2021*. https://doi.org/10.1109/ISCAS51556.2021.9401211

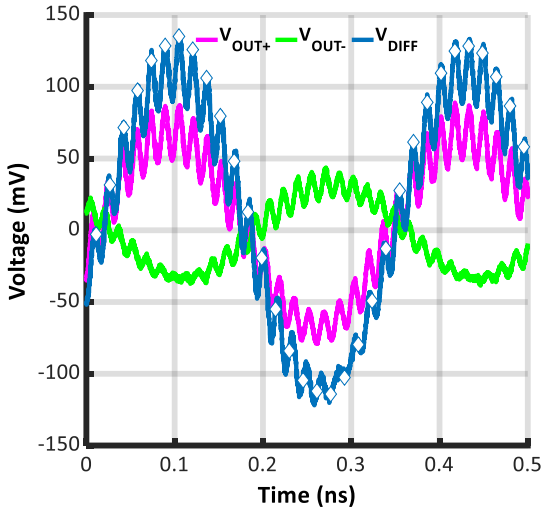
64 GS/s Voltage Mode Sampler (2)

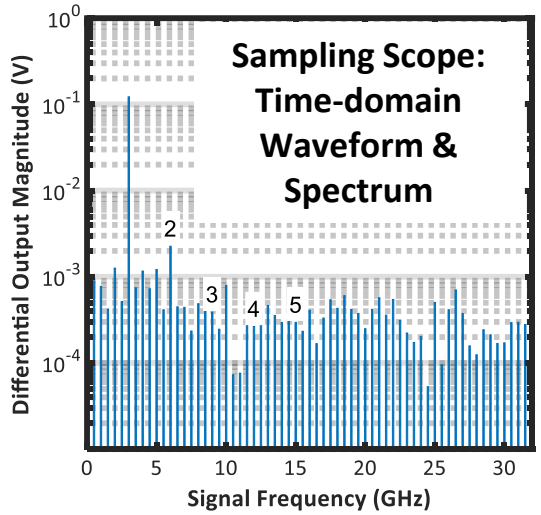
Sampler Core Layout



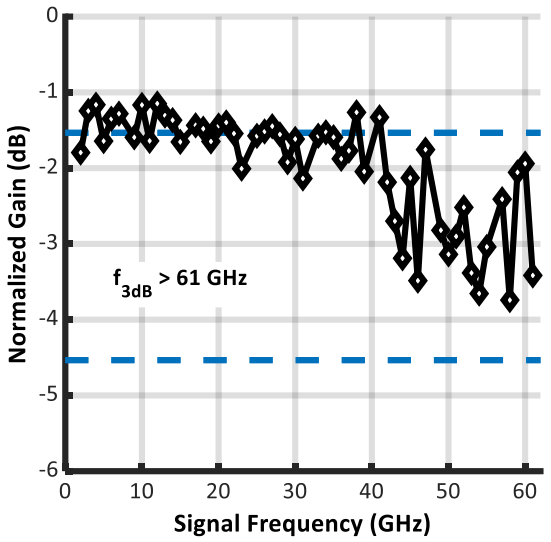
Chip Photograph

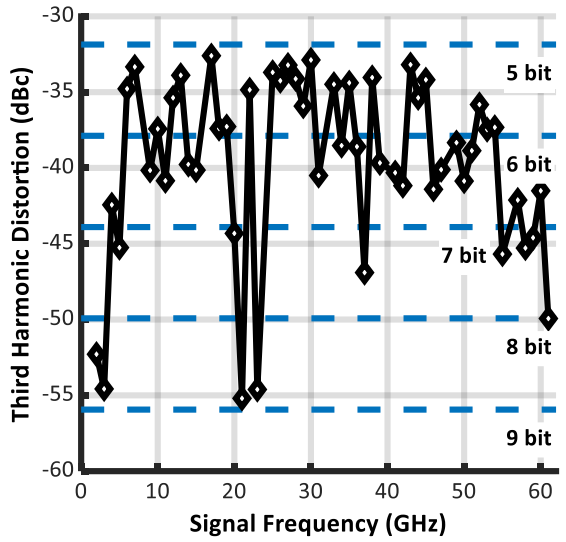






Sampler Frequency Response & THD





Param.	Spec.	Sim.	Meas.
f_S	40 GS/s	51.2 GS/s	**64 GS/s**
f_{in}	55 GHz	75 GHz	**> 61 GHz**
ENOB	3 bit	6.5 bit	**5.0 bit**
P_{DC}	1.5 W	1.6 W	**1.5 W**

P. Thomas, M. Grözing, and M. Berroth, "64-GS/s 6-bit Track-and-Hold Circuit with More Than 61 GHz Bandwidth at 1.0 V pp Input Voltage Swing in 90-nm SiGe BiCMOS Technology," *ISCAS 2021*. https://doi.org/10.1109/ISCAS51556.2021.9401211

64 GS/s VM Sampler: Comparison (2020)

- Advanced 90-nm SiGe-BiCMOS technology → **64 GS/s at 1.0 V_{pp}** input voltage swing
- Linearized preamplifier → **ultra-high bandwidth** covering 1st & 2nd Nyquist band
- Linearized switched emitter follower → accuracy suitable for **6–8-bit ADCs**

Ref.	Sampling Rate	Analog Input Bandwidth	Third Harmonic Distortion	Diff. Input Voltage Swing	Total / Core Power Consumption	Total / Core Active Area	Technology f_T / f_{max}
[1]	32 GS/s	58 GHz (large-signal)	-64 dBc to -29 dBc (2 – 61 GHz)	1.0 V_{pp}	1.8 W / 685 mW	1.5 / 0.044 mm²	130-nm SiGe 250 / 400 GHz
[2]	40 GS/s **+100%**	70 GHz	-48 dBc to -32 dBc (1–19 GHz)	0.45 V_{pp}	— / 440 mW	0.72 / 0.046 mm²	130-nm SiGe 300 / 500 GHz
[3]	70 GS/s / 60 GS/s [1]	51 GHz	-52 dBc to -37 dBc (0–15 GHz)	0.4 V_{pp}	1.9 W / —	1.8 mm² / —	700-nm InP 320 GHz / —
[4]	108 GS/s / 90 GS/s [2]	40 GHz	-44 dBc to -34 dBc (20 & 40 GHz)	0.4 V_{pp}	0.09 W / 20 mW	0.489 / 0.018 mm²	55-nm SiGe 330 / 350 GHz
This Work	**64 GS/s**	**>61 GHz (large-signal)**	**-45 dBc to -32 dBc (2 – 50 GHz)**	**1.0 V_{pp}**	**1.5 W / 465 mW**	**1.5 / 0.023 mm²**	**90-nm SiGe 300 / 480 GHz**

[1] Max. sampling rate 70 GS/s, linearity measured at 60 GS/s.
[2] Max. sampling rate 108 GS/s, linearity measured at 90 GS/s.

-17% / -32% **-48%** **Technology advancement**

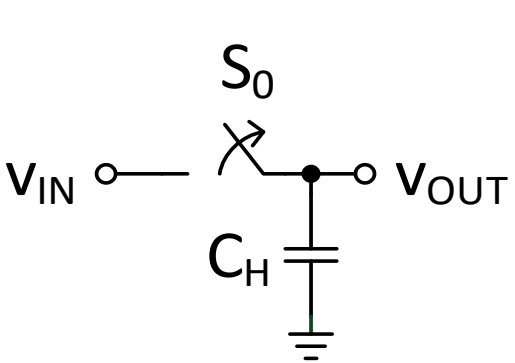
- Operational in **2 full Nyquist bands** → extension to a 1:2 analog demultiplexer possible
- Frequency conversion above Nyquist rate → bandwidth "gearbox" for CMOS ADCs
- Time-interleaved sampling system → **next-gen. Rx with > 200 Gbit/s @ > 100 Gbaud**

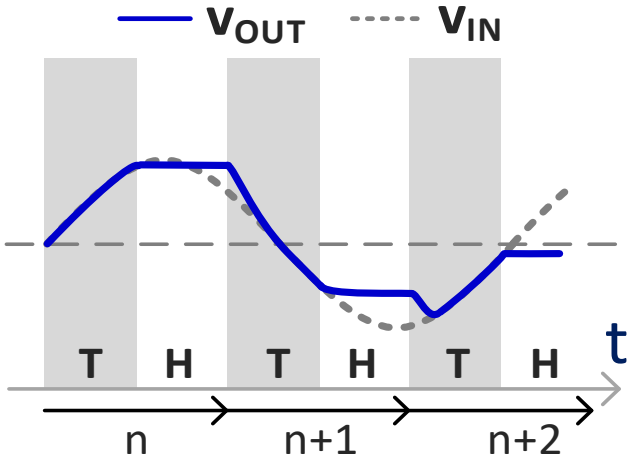
[1] P. Thomas, M. Grözing, and M. Berroth, "32-GS/s SiGe track-and-hold amplifier with 58-GHz bandwidth and -64-dBc to -29-dBc HD3," ICECS 2020.
[2] L. Wu, M. Weizel, and J. C. Scheytt, "A 70 GHz small-signal bandwidth 40 GS/s track-and-hold amplifier in 130 nm SiGe BiCMOS technology," ICECS 2019.
[3] J. Deza, A. Ouslimani, A. Konczykowska, A. Kasbari, J. Godin, and G. Pailler, "70 GSa/s and 51 GHz bandwidth track-and-hold amplifier in InP DHBT process," Electron. Lett., vol. 49, no. 6, pp. 388–389, Mar. 2013.
[4] K. Vasilakopoulos, A. Cathelin, P. Chevalier, T. Nguyen, and S. P. Voinigescu, "A 108GS/s track and hold amplifier with MOS-HBT switch,", IMS 2016.
P. Thomas, M. Grözing, and M. Berroth, "64-GS/s 6-bit Track-and-Hold Circuit …," *ISCAS 2021.* https://doi.org/10.1109/ISCAS51556.2021.9401211

High-Bandwidth
Analog-to-Digital-Converter Front-Ends
in SiGe-BiCMOS Technology

Voltage Mode versus Current / Charge Mode Sampling

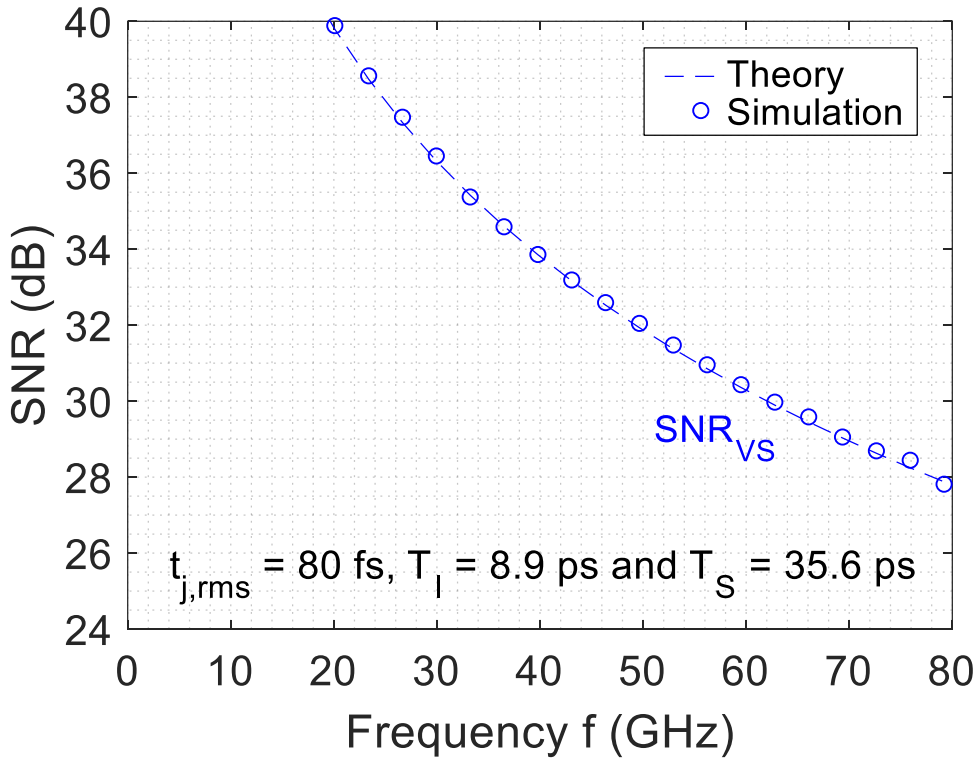
Voltage Mode Sampling





T = Track, H = Hold

Voltage Sampling



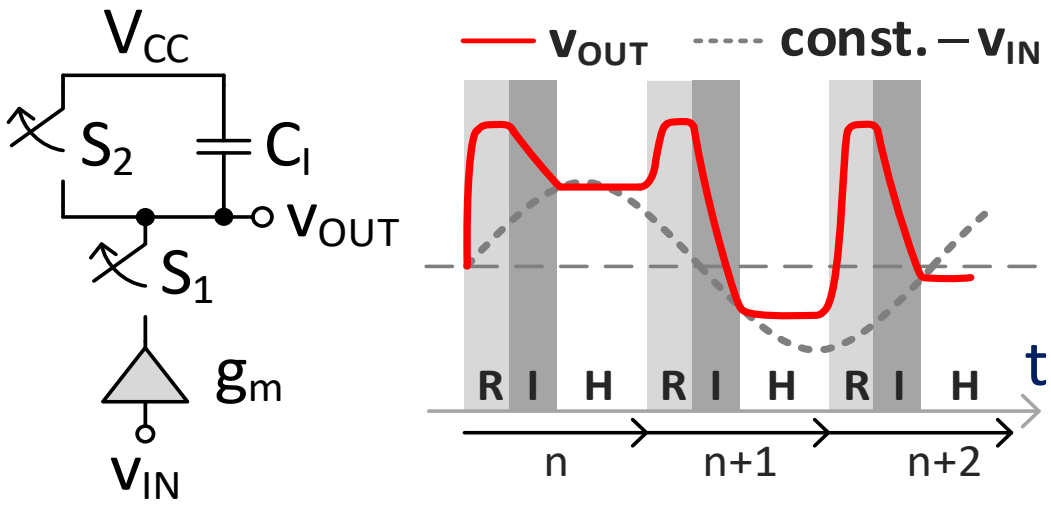
$$SNR_{VS} = \left(\frac{1}{2\pi f t_{j,rms}}\right)^2$$

$t_{j,rms}$ … root mean square (rms) sampling clock jitter

Voltage Sampling: SNR is restricted by rms sampling clock jitter at high input frequencies

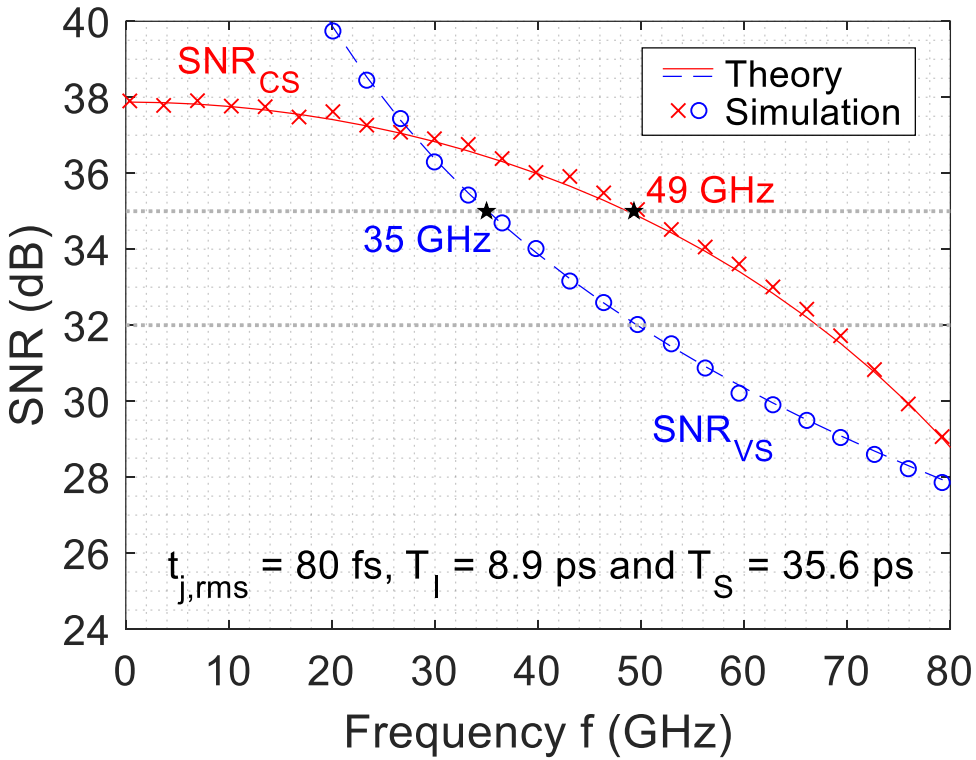
X-.Q. Du, M. Grözing et al. “A 112-GS/s 1-to-4 ADC front-end with more than 35dBc SFDR and 28dB SNDR up to 43GHz in 130nm SiGe BiCMOS,” RFIC 2019. https://doi.org/10.1109/RFIC.2019.8701786

Current Mode / Charge Sampling



R = Reset, I = Integration, H = Hold

Charge Sampling



$$SNR_{CS} = \left(\frac{\sqrt{1 - \cos(2\pi f T_I)}}{2\pi f t_{j,rms}} \right)^2$$

$t_{j,rms}$ … root mean square (rms) sampling clock jitter
T_I … mean integration period

Charge Sampling enables up to 3 dB SNR improvement for $f > \frac{1}{4T_I}$ for the same rms clk jitter

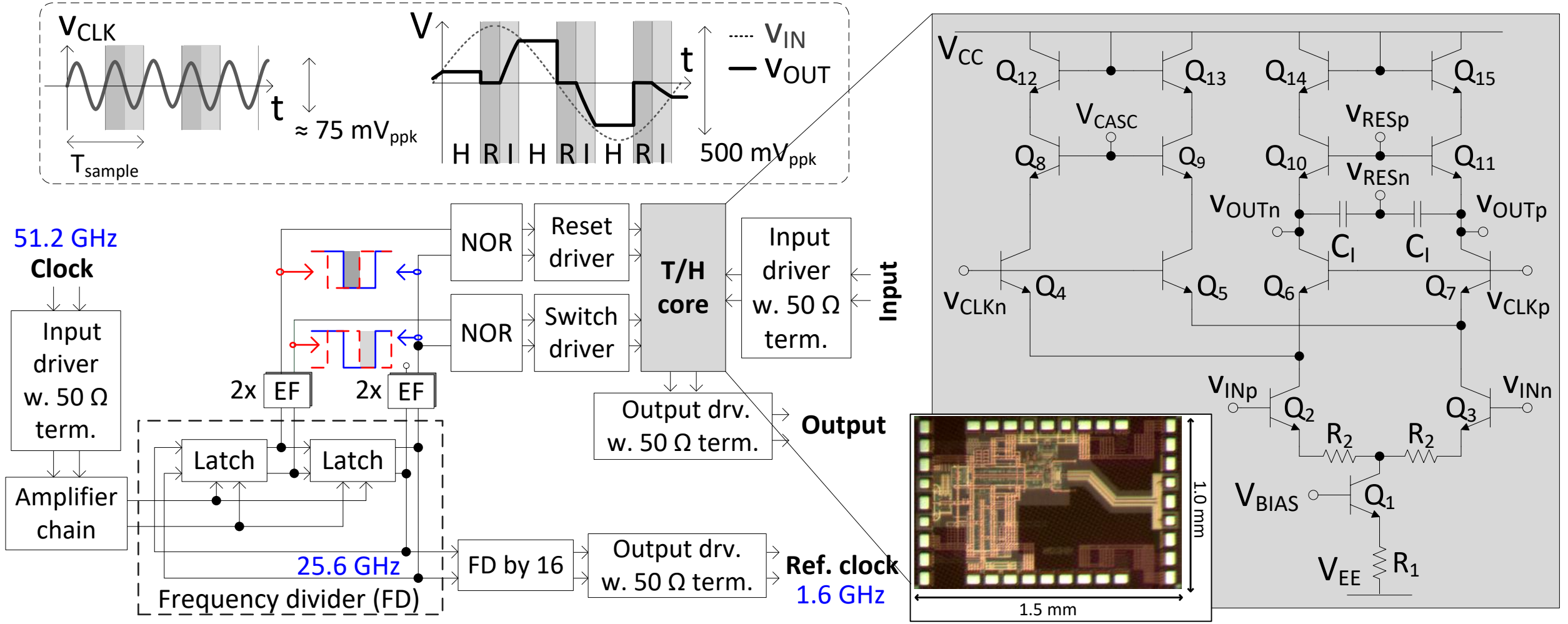
X-.Q. Du, M. Grözing et al. "A 112-GS/s 1-to-4 ADC front-end with more than 35dBc SFDR and 28dB SNDR up to 43GHz in 130nm SiGe BiCMOS," RFIC 2019. https://doi.org/10.1109/RFIC.2019.8701786

High-Bandwidth
Analog-to-Digital-Converter Front-Ends
in SiGe-BiCMOS Technology

25 GS/s 40-GHz-1dB-Bandwidth Current Mode Track&Hold Circuit

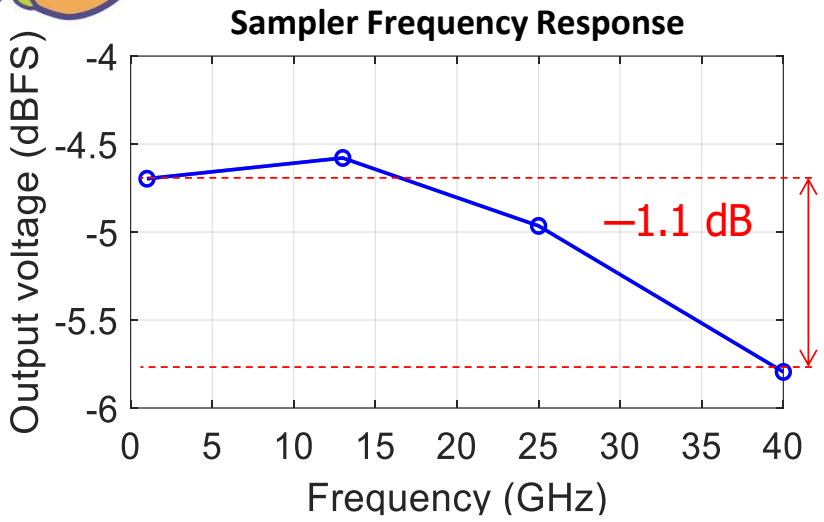
25-GS/s Current Mode Sampler (1)

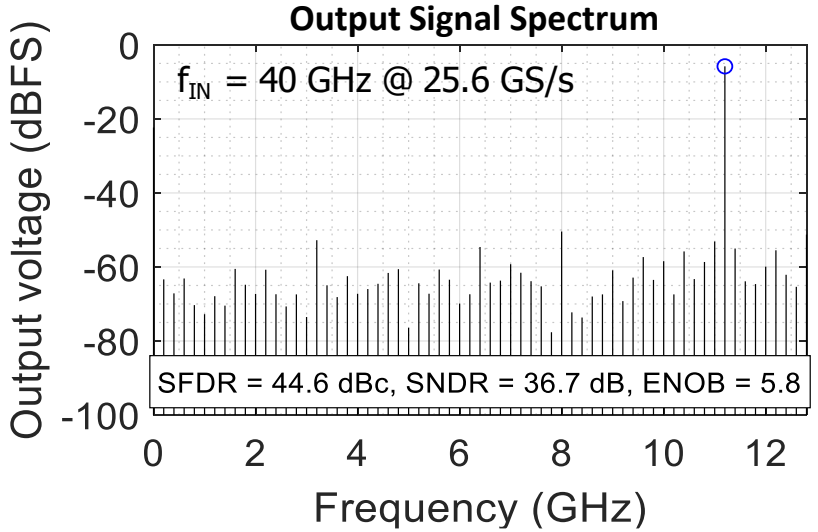
CM-TH Block Diagram and Core Schematic

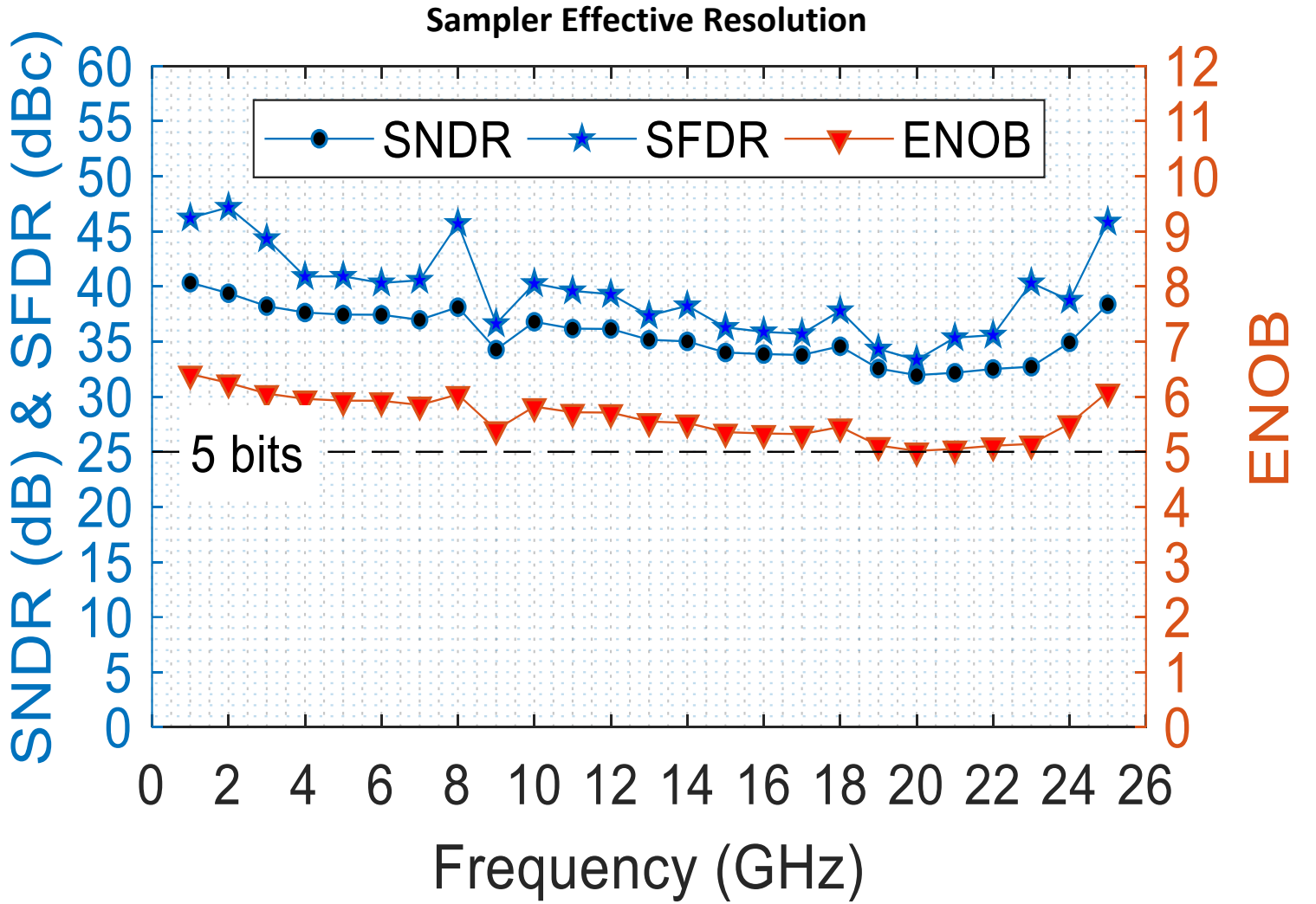


X.-Q. Du, M. Grözing, M. Berroth, "A 25.6-GS/s 40-GHz 1-dB BW Current-Mode Track and Hold Circuit with more than 5-ENOB," *BCICTS 2018.* https://doi.org/10.1109/BCICTS.2018.8550855

25-GS/s Current Mode Sampler (2)







X.-Q. Du, M. Grözing, M. Berroth, "A 25.6-GS/s 40-GHz 1-dB BW Current-Mode Track and Hold Circuit with more than 5-ENOB," *BCICTS 2018.* https://doi.org/10.1109/BCICTS.2018.8550855

25-GS/s CM Sampler: Comparison (2018)

	[1]	[2]	This work
Sampling topology	Switched capacitor	Switched emitter follower	Charge-sampling
P_{in} (dBm)	−4 (=0.4 V_{ppk})	−4 (=0.4 V_{ppk})	−2 (=0.5 V_{ppk})
f_{sample} (GHz)	25	60	25.6
BW (GHz)	55 (3-dB BW)	51 (3-dB BW)	40 (1-dB BW)
Gain (dB)	−11.5	−7.5 (−1.5 diff.)	−2.8
SNDR/THD (dB/dB) @f_{in} (GHz)	31/−37 @ 3 30.5/−36 @14.8 30/−33 @26.5 29/−32 @49.8	N/A/−52 @ 2 N/A/−37 @15	40.0/−44.2 @ 1 35.3/−35.9 @13 38.1/−42.6 @25 36.7/−39.4 @40
P_{DC}(mW)	73	1850	913
Die area (mm^2)	0.53	1.8	1.5
Technology f_T/f_{max} (GHz/GHz)	28 nm CMOS Low Power	700 nm InP DHBT 320/380	130 nm SiGe BiCMOS 250/400

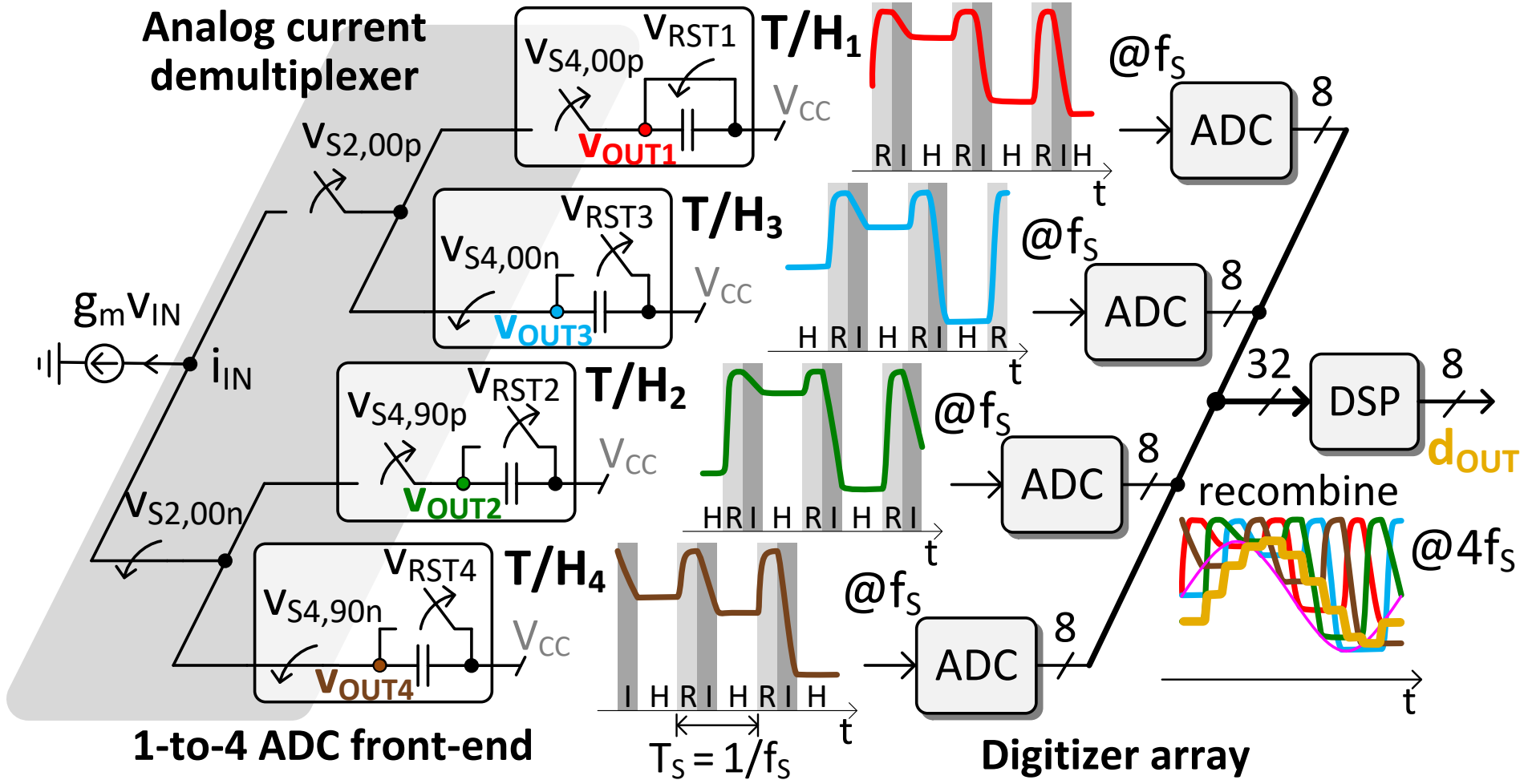
[1] G. Tretter, D. Fritsche, M. M. Khafaji, C. Carta and F. Ellinger, "A 55-GHz-Bandwidth Track-and-Hold Amplifier in 28-nm Low-Power CMOS," in *IEEE TCAS-II: Express Briefs*, vol. 63, no. 3, pp. 229-233, Mar. 2016.
[2] J. Deza, A. Ouslimani, A. Konczykowska, A. Kasbari, J. Godin and G. Pailler, "70 GSa/s and 51 GHz bandwidth track-andhold amplifier in InP DHBT process," in *Electronics Letters*, vol. 49, no. 6, pp. 388-389, Mar. 2013.

X.-Q. Du, M. Grözing, M. Berroth, "A 25.6-GS/s 40-GHz 1-dB BW Current-Mode Track and Hold Circuit with more than 5-ENOB," *BCICTS 2018.* https://doi.org/10.1109/BCICTS.2018.8550855

High-Bandwidth
Analog-to-Digital-Converter Front-Ends
in SiGe-BiCMOS Technology

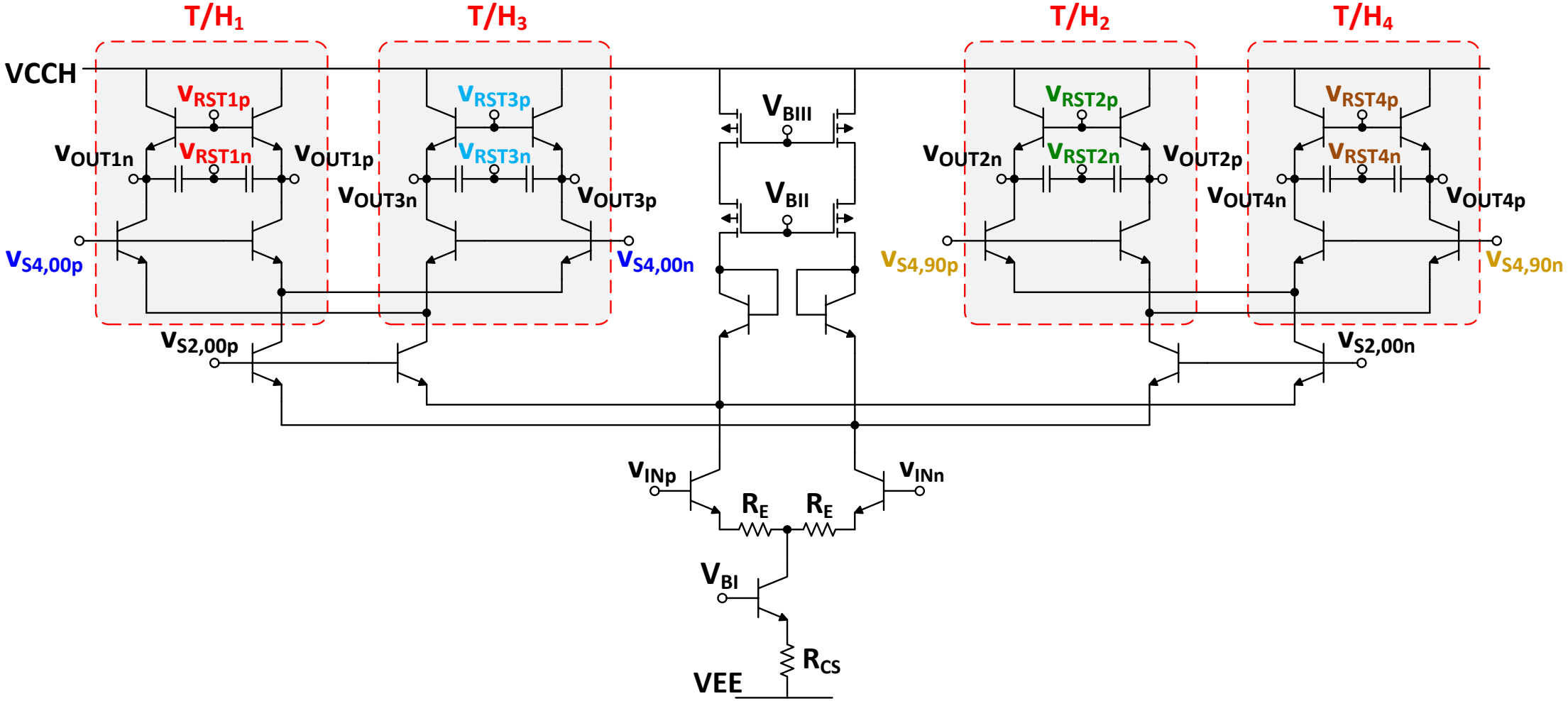
112 GS/s & 128 GS/s Current Mode 1:4 Analog Demultiplexer Circuits

1:4 ADeMUX: Operation Principle



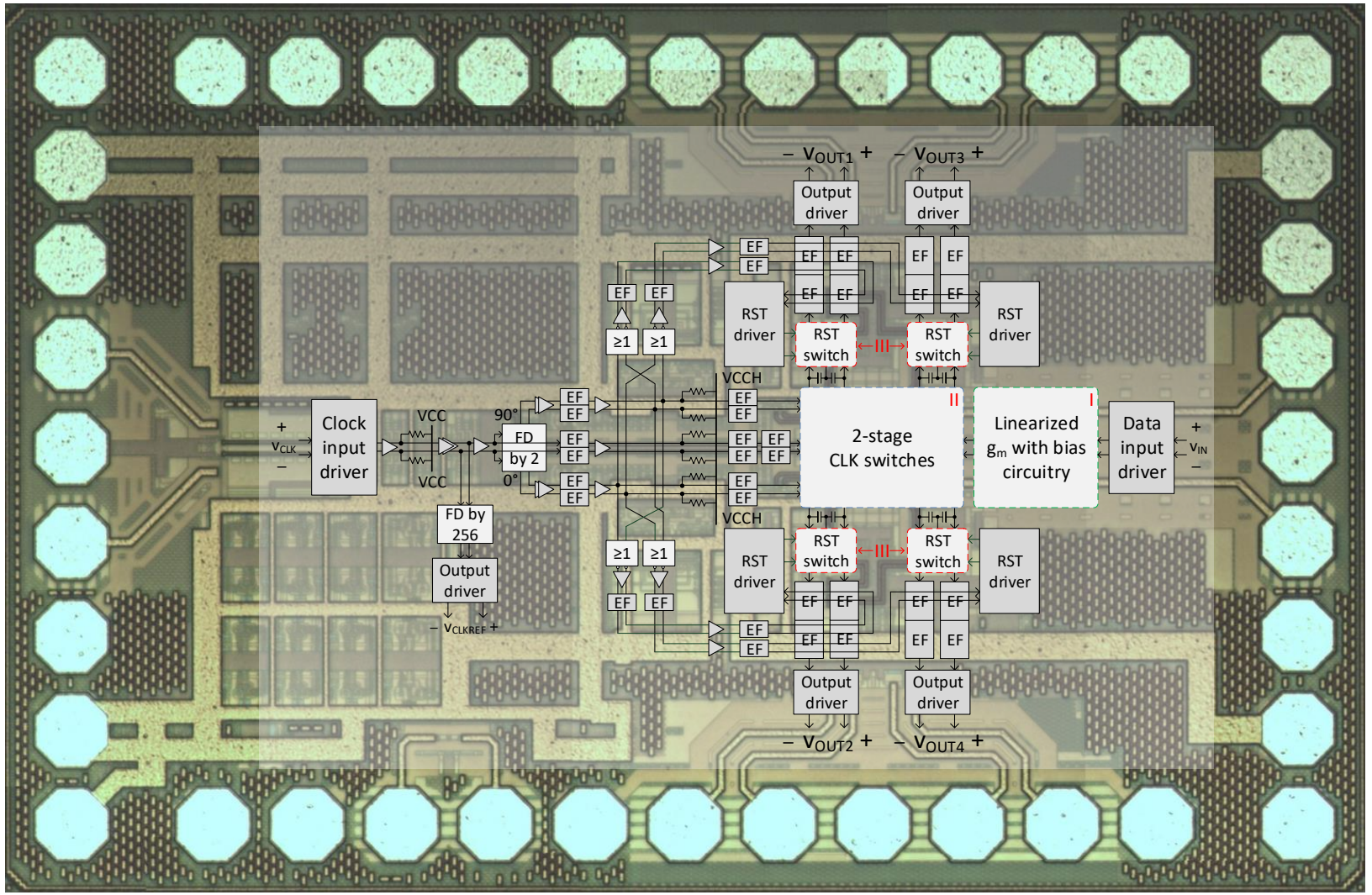
X.-Q. Du, M. Grözing, A. Uhl, S. Park, F. Buchali, K. Schuh, and M. Berroth,
"A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," *RFIC 2019.* https://doi.org/10.1109/RFIC.2019.8701786

112 GS/s 1:4 ADeMUX: Core Schematic



X.-Q. Du, M. Grözing, A. Uhl, S. Park, F. Buchali, K. Schuh, and M. Berroth,
"A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," *RFIC 2019.* https://doi.org/10.1109/RFIC.2019.8701786

112 GS/s ADeMUX: Block Diagram & Layout



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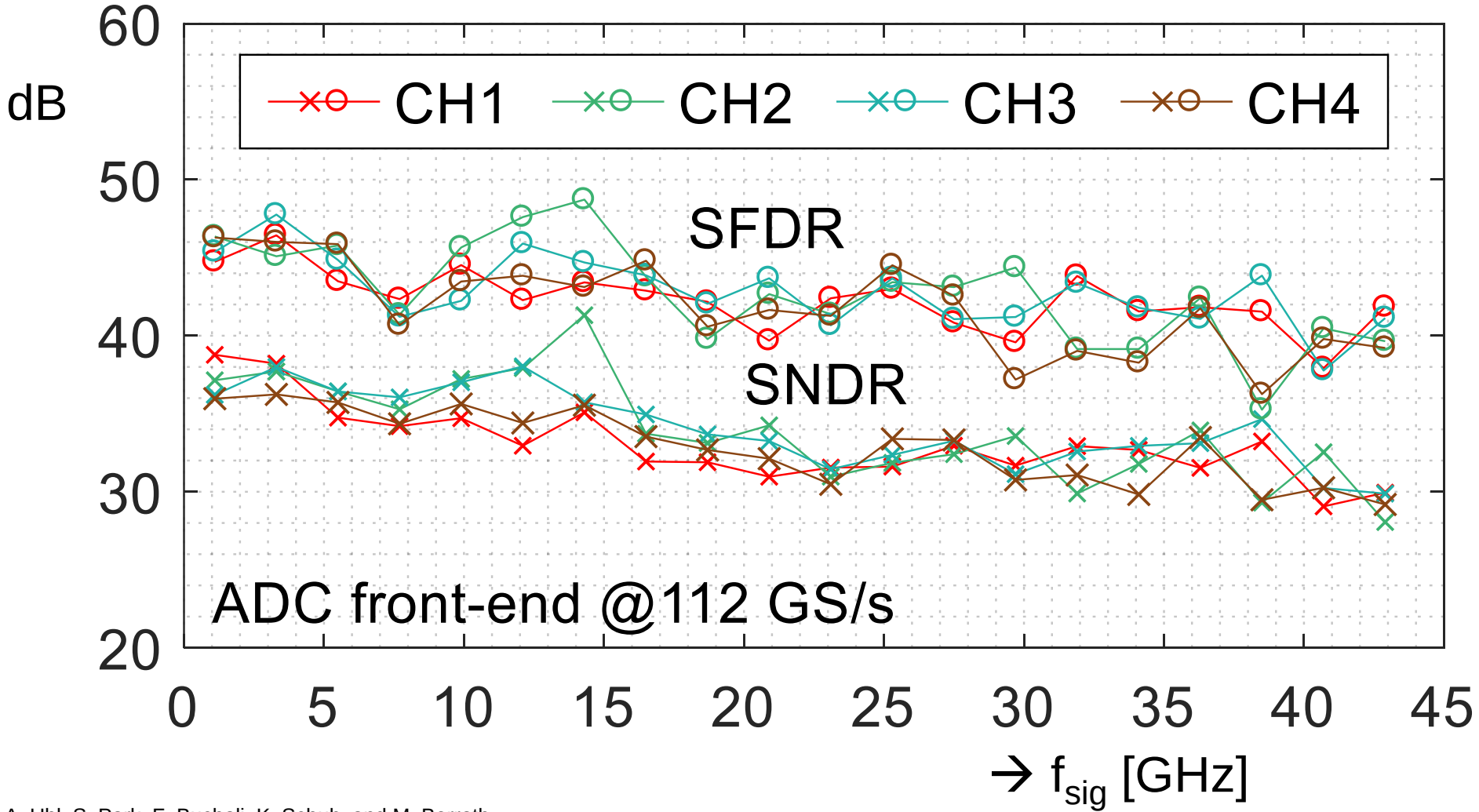
"A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," *RFIC 2019.* https://doi.org/10.1109/RFIC.2019.8701786

112 GS/s ADeMUX: SFDR & SNDR (Meas.)



X.-Q. Du, M. Grözing, A. Uhl, S. Park, F. Buchali, K. Schuh, and M. Berroth,
"A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," *RFIC 2019.* https://doi.org/10.1109/RFIC.2019.8701786

112 GS/s ADeMUX: Summary & Comparison (2019)

Time-interleaved samplers enabling ≥100 GBd PAM-4 reception

Parameter	This work	DSO [1]	DSO [2]
Sample rate (GS/s)	112 4x28	160	256 4x64
Frequency range (GHz)	DC–50	DC–63	DC–110
Technology	SiGe BiCMOS f_T = 300 GHz	InP	InP f_T = 600-700 GHz*
PAM-4 Baudrates	100 GBd 40 km SMF [3]	107 GBd 10 km SMF [4]	160 GBd 10 km SMF [5]

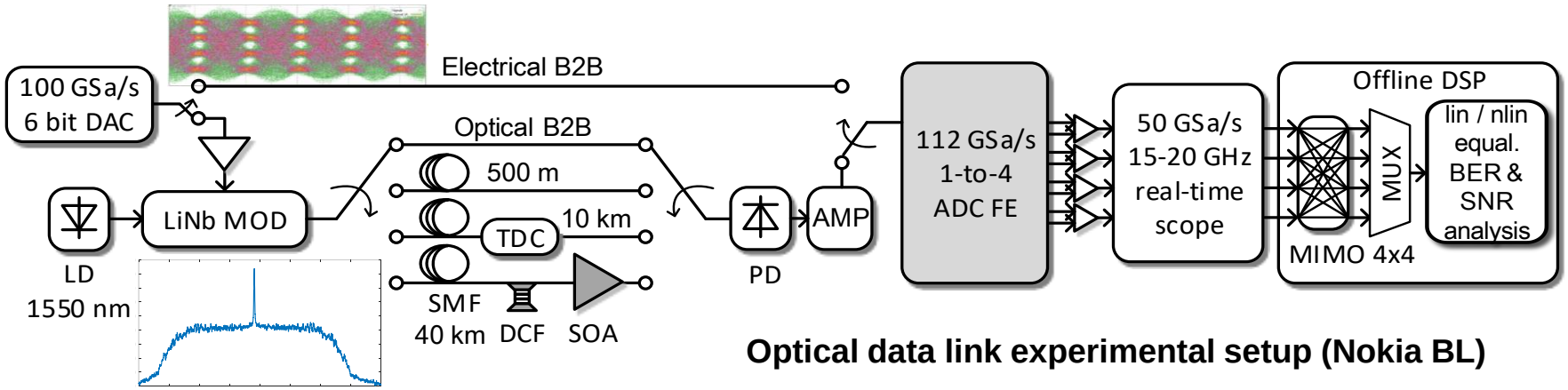
[1] Data sheet: https://prc.keysight.com/Content/PDF_Files/5991-3868EN.pdf
[2] Data sheet: https://literature.cdn.keysight.com/litweb/pdf/5992-3132EN.pdf
[3] F. Buchali *et al.*, "A SiGe HBT BiCMOS 1-to-4 ADC Frontend Supporting 100 GBaud PAM4 Reception at 14 GHz Digitizer Bandwidth," *OFC 2019*, Paper Th4A7.
[4] S. Kanazawa *et al.*, "Transmission of 214-Gbit/s 4-PAM signal using an ultra-broadband lumped-electrode EADFB laser module," *OFC 2016*, Paper Th5B.3.
[5] H. Yamazaki *et al.*, "160-GBd (320-Gb/s) PAM4 Transmission Using 97-GHz Bandwidth Analog Multiplexer," *IEEE Photonics Technology Letters*, vol. 30, no. 20, pp. 1749-1751, Oct.15, 2018.

*https://www.youtube.com/watch?v=DXYje2B04xE

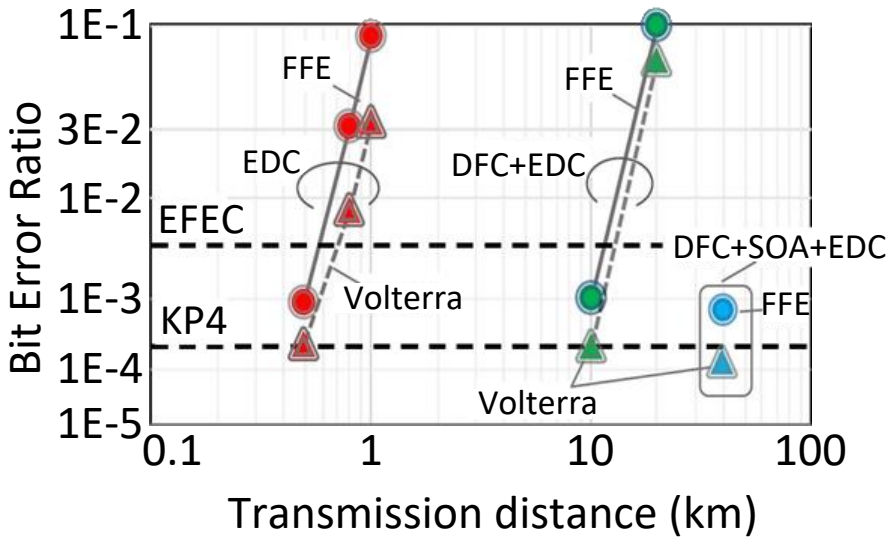
First SiGe BiCMOS sampler for 100 GBd PAM-4 reception demonstrated

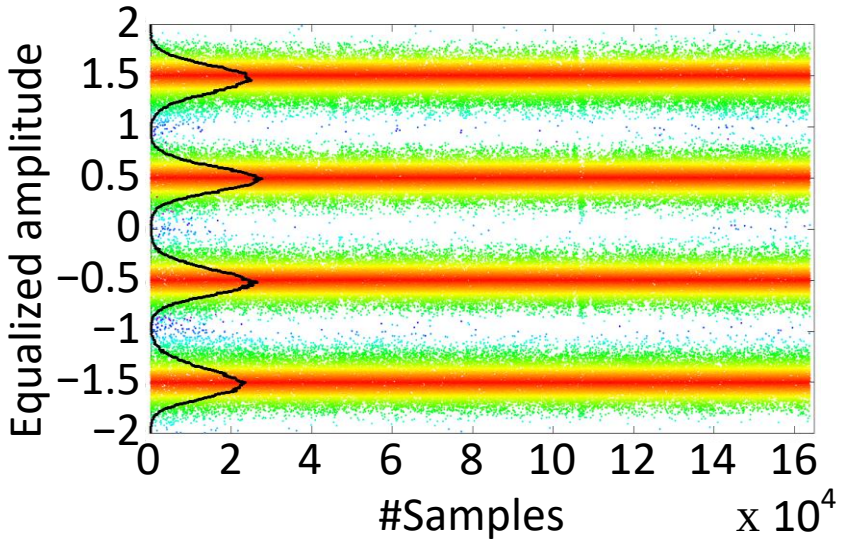
X.-Q. Du, M. Grözing, A. Uhl, S. Park, F. Buchali, K. Schuh, and M. Berroth,
"A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," *RFIC 2019.* https://doi.org/10.1109/RFIC.2019.8701786

112 GS/s ADeMUX: Optical Rx Application



Optical data link experimental setup (Nokia BL)



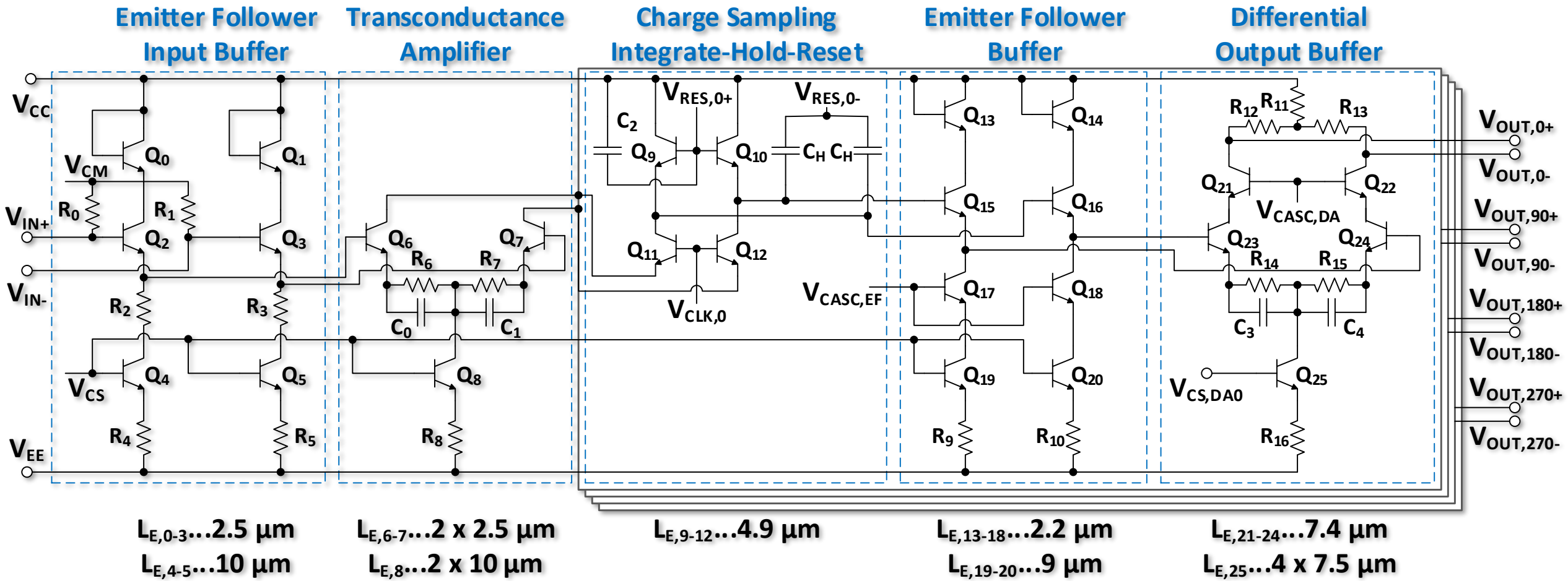


100 GBd PAM-4 with BER < EFEC threshold with linear EQ & BER < KP4 threshold with Volterra EQ (Nokia BL)

F. Buchali, X.-Q. Du, M. Grözing *et al.*, "A SiGe HBT BiCMOS 1-to-4 ADC Frontend Supporting 100 GBaud PAM4 Reception at 14 GHz Digitizer Bandwidth," OFC 2019. https://doi.org/10.1364/OFC.2019.Th4A.7

128 GS/s 1:4 ADeMUX (1)

1:4 CM-ADeMUX Signal Path Schematic



$L_{E,0\text{-}3}$...2.5 µm
$L_{E,4\text{-}5}$...10 µm

$L_{E,6\text{-}7}$...2 x 2.5 µm
$L_{E,8}$...2 x 10 µm

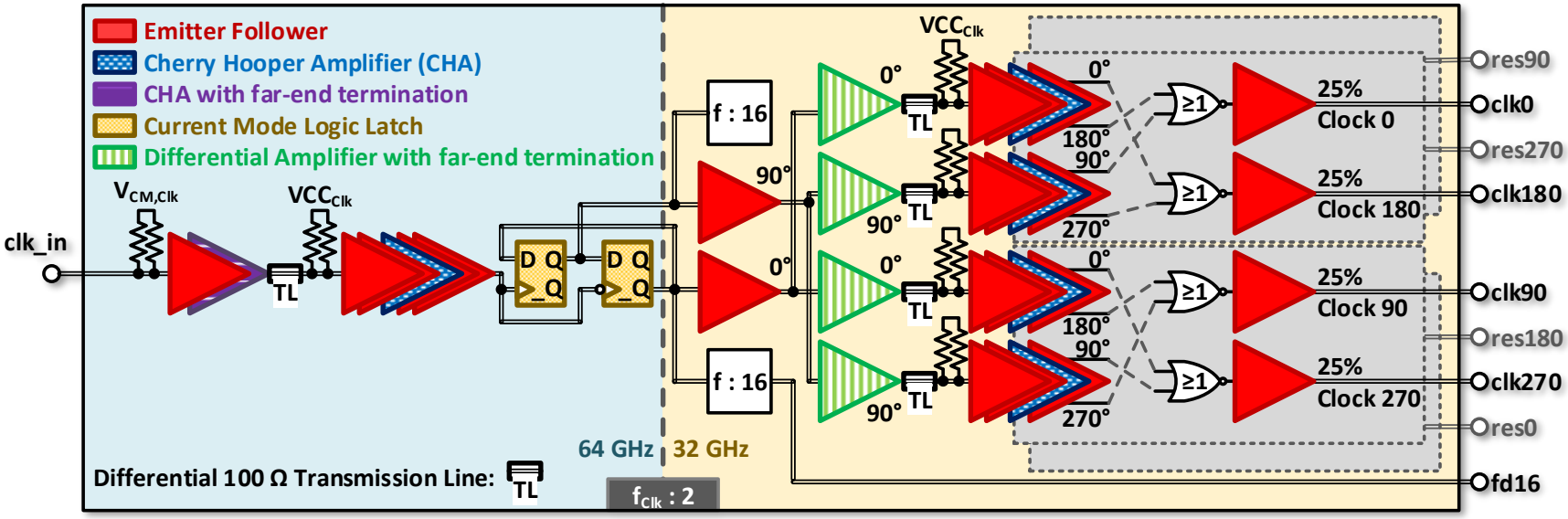
$L_{E,9\text{-}12}$...4.9 µm

$L_{E,13\text{-}18}$...2.2 µm
$L_{E,19\text{-}20}$...9 µm

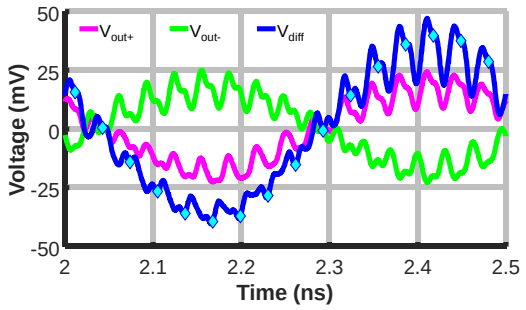
$L_{E,21\text{-}24}$...7.4 µm
$L_{E,25}$...4 x 7.5 µm

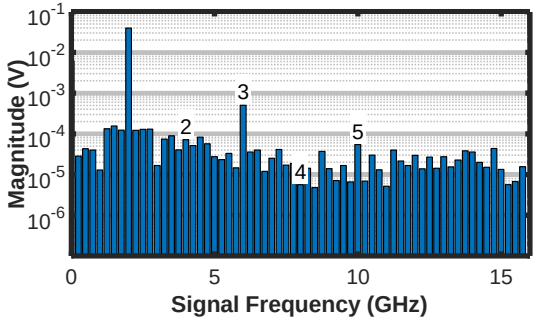
P. Thomas, T. Tannert, M. Grözing, and M. Berroth, "128-GS/s 1-to-4 SiGe Analog Demultiplexer with 36-GHz Bandwidth for 6-bit Data Converters," *BCICTS 2020.* https://doi.org/10.1109/BCICTS48439.2020.9392964

128 GS/s 1:4 ADeMUX (2)



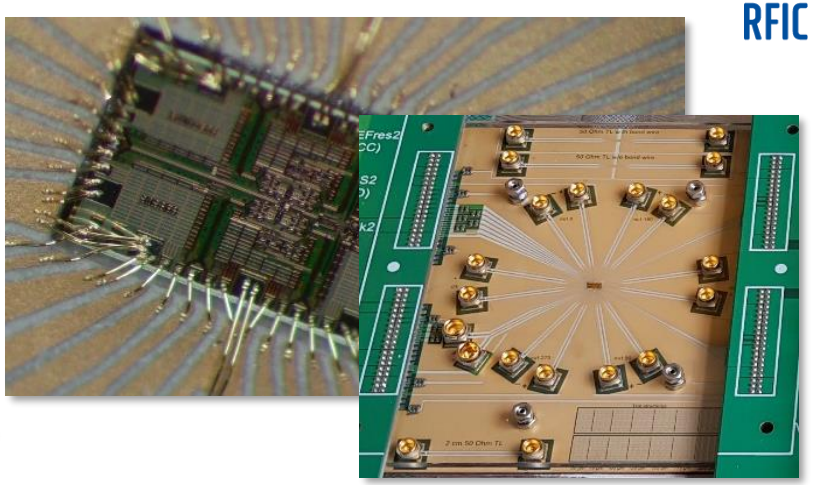
Clock Path Block Diagram



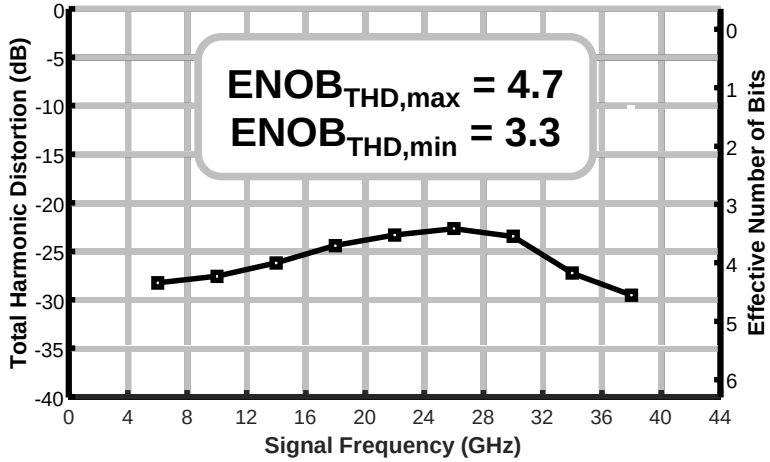


Sampling Scope Time Domain Measurement and Signal Spectrum

Param.	Spec.	Sim.	Meas.
f_S	108 GS/s	128 GS/s	**128 GS/s**
$f_{in,3dB}$	55 GHz	66 GHz	**36 GHz**
ENOB	3 bit	4.8 bit	**3.3 bit**
P_{DC}	4.0 W	3.7 W	**2.6 W**



Chip and RF Board Photographs



THD and Effective Resolution

P. Thomas, T. Tannert, M. Grözing, and M. Berroth, "128-GS/s 1-to-4 SiGe Analog Demultiplexer with 36-GHz Bandwidth for 6-bit Data Converters," *BCICTS 2020*. https://doi.org/10.1109/BCICTS48439.2020.9392964

128 GS/s 1:4 ADeMUX: Comparison (2020)

- Highest reported sampling rate for analog front-ends, as in [1]
- More energy-efficient than earlier current-mode ADeMUX [2,3]
- Large power consumption of clock conditioning still an issue

Ref.	Sampling Rate	Bandwidth	Peak-Peak Input Voltage Swing	Spurious-Free Dynamic Range	Total Harmonic Distortion	Total / Core DC Power	Supply Voltage	Technology f_T / f_{max}
[2]	4 x 28 GS/s = 112 GS/s	–	500 mV	44 dBc @ 1 GHz 35 dBc @ 38 GHz	-46 dB @ 1 GHz [a] -35 dB @ 43 GHz [a]	3.34 W / 2.28 W	3.5 V / 6.5 V	130-nm SiGe 300 / 450 GHz
[3]	4 x 29 GS/s = 116 GS/s	–	500 mV	44 dBc @ 2 GHz 29 dBc @ 27 GHz	-41 dB @ 2 GHz -28 dB @ 27 GHz	5.5 W / 1.8 W	4.7 V / 4.6 V	130-nm SiGe 250 / 400 GHz
[4]	108 GS/s / 90 GS/s [b]	40 GHz [c]	800 mV	55 dBc @ 1 GHz 43 dBc @ 15 GHz	-49 dB @ 1 GHz -38 dB @ 15 GHz	0.09 W / 0.02 W	2.5 V / 1.8 V	55-nm SiGe 330 / 350 GHz
This Work	4 x 32 GS/s = 128 GS/s	36 GHz	500 mV	38 dBc @ 2 GHz 30 dBc @ 30 GHz	-37 dB @ 2 GHz -22 dB @ 26 GHz	2.59 W / 0.43 W	3.6 V / 3.1 V	90-nm SiGe 300 / 480 GHz

a. Assuming THD = –SNDR. b. Max. sampling rate 108 GS/s, linearity measured at 90 GS/s. c. Track mode bandwidth.

[1] A. Zandieh *et al.*, „128-GS/s ADC front-end with over 60-GHz input bandwidth in 22-nm Si/SiGe FDSOI CMOS“, in *BCICTS* 2018.
[2] X.-Q. Du *et al.*, „A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS“, in *RFIC* 2019.
[3] P. Thomas *et al.*, „A 1-to-4 SiGe BiCMOS analog demultiplexer sampling front-end for a 116 Gbaud-receiver“, in *EuMIC* 2020.
[4] K. Vasilakopoulos *et al.*, „A 108GS/s track and hold amplifier with MOS-HBT switch“, in *IMS* 2016.

P. Thomas, T. Tannert, M. Grözing, and M. Berroth, “128-GS/s 1-to-4 SiGe Analog Demultiplexer with 36-GHz Bandwidth for 6-bit Data Converters,” *BCICTS 2020.* https://doi.org/10.1109/BCICTS48439.2020.9392964

Conclusion

- Comparison between Current-Mode and Voltage Mode Sampling
- Front-Ends for Single-Channel ADC
  - 40 GS/s without Track&Hold Circuit
  - 64 GS/s Voltage Mode Track&Hold Circuit (Switched Emitter Follower)
  - 25 GS/s Current Mode Track&Hold Circuit (Charge Sampling)
- 1:4 Analog Demultiplexer Front-Ends for Time-Interleaved-ADCs
  - 112 GS/s ADeMUX
  - 128 GS/s ADeMUX

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6. F. Buchali, K. Schuh, S. T. Le, X.-Q. Du, M. Grözing, and M. Berroth, "A SiGe HBT BiCMOS 1-to-4 ADC frontend supporting 100 GBaud PAM4 reception at 14 GHz digitizer bandwidth," in *2019 Optical Fiber Communication Conference (OFC 2019)*, 2019. https://doi.org/10.1364/OFC.2019.Th4A.7
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