20.10.2021

This manuscript is accepted for publication at

2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA, USA, December 6–9, 2021.

Analog Demultiplexer Operating at up to 200 GS/s Using Four Time Interleaved Switched Emitter Followers with a 50% Duty Cycle Clock

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***Abstract*—This paper presents the design and experimental results of a voltage mode analog demultiplexer (ADeMUX) that uses four time interleaved switched emitter follower track-and-hold (T/H) circuits. The preamplifiers and sampling cores are linearized for ultra-broadband operation. With the utilized 90-nm SiGe-BiCMOS technology offering 300 GHz f_T and 480 GHz f_{max}, we are able to operate the ADeMUX with up to 4 x 50 GS/s = 200 GS/s – the highest reported sampling rate to date. Compared with the state-of-the-art current mode ADeMUX circuits, the presented device offers an increase in sampling rate of more than 50%. At 128 GS/s, the chip shows the highest input bandwidth of more than 50 GHz and a linearity of more than 3 bit. This ultra-broadband analog time interleaver can be used to feed four analog-to-digital converters in CMOS technology, due to the reduced bandwidth requirement of only 16 GHz for operation at 128 GS/s or 25 GHz for 200 GS/s.**

Keywords—Analog-to-digital conversion, BiCMOS integrated circuits, demultiplexing, sampled data circuits, silicon germanium, switched emitter follower.

I. Introduction

State-of-the-art analog-to-digital converters (ADC) are realized in 5-nm or 7-nm CMOS technology, which offers ultra-high density integration and new on-chip functionality. For the digital signal processor (DSP) of optical modules, this means that additional channel equalization, error correction, and signal shaping can be integrated on the same silicon die [1]. To increase single-lane data rates beyond 100 Gbit/s, more complex modulation formats or higher symbol rates are required, the latter increasing the required ADC bandwidth. In the smallest CMOS nodes, ADCs experience severe bandwidth limitations and are prone to increasing mismatch and quantum effects. SiGe-BiCMOS technologies offer higher transistor cut-off frequencies with larger transistor structures, where processes can still be reasonably well controlled for superior analog performance. Compared to faster III-V compound semiconductor technologies like InP, SiGe circuits can be processed on more cost-efficient 200-mm and 300-mm wafers, making the technology attractive to cost-sensitive applications like optical transceivers. However, challenges of hybrid integration in multi-chip modules (MCM) must be overcome, to realize compact form factors.

This work was supported in part by the European Union within the ECSEL-JU H2020 Project TARANTO under Grant 737454, in part by the German Federal Ministry of Education and Research under Grant 16ESE0210, and in part by the German Research Foundation within the Priority Program SPP 2111: Electronic-Photonic Integrated Systems for Ultrafast Signal Processing under Grant BE 2256/34-1.

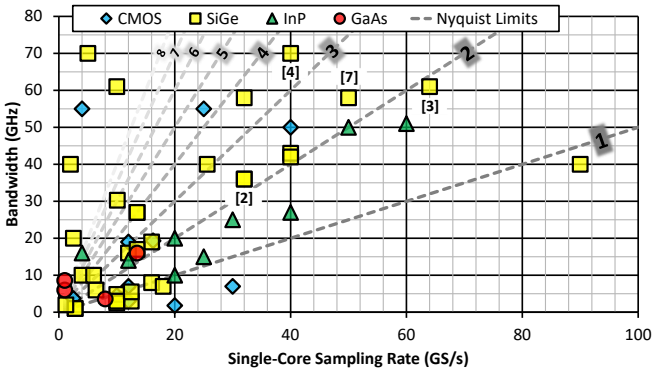
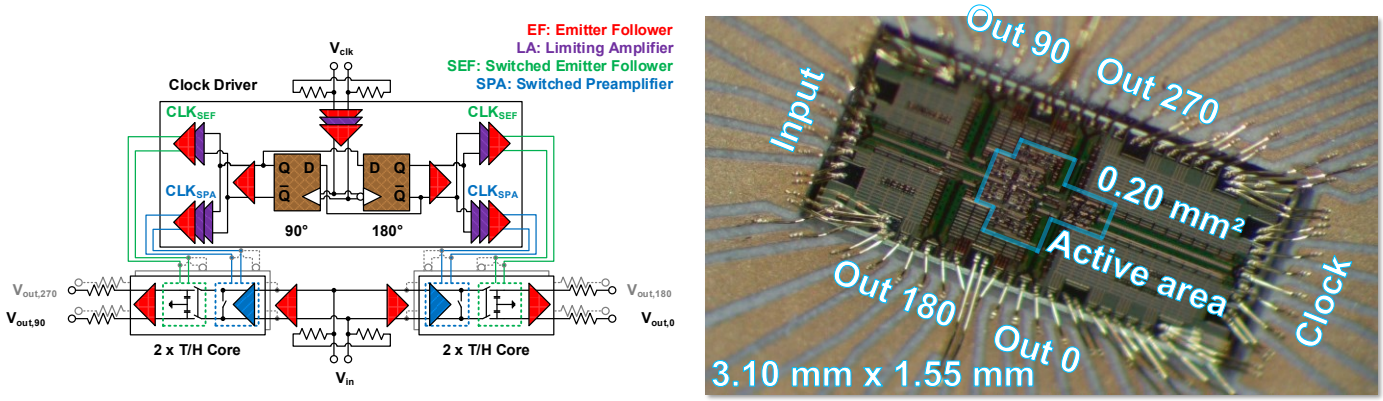


Fig. 1. Overview of the sampling rate, input bandwidth, and the number of Nyquist zones covered by state-of-the-art sampling front ends in the Gigasample-range.

A time interleaving front end like an analog demultiplexer (ADeMUX) can utilize the high analog performance of a SiGe-BiCMOS technology, combined with a densely integrated CMOS DSP. State-of-the-art CMOS ADCs can support symbol rates of up to 66 Gbaud [1], whereas up to 128 Gbaud were demonstrated in a 1-to-4 SiGe-ADeMUX using current mode track-and-hold (T/H) circuits [2]. The current mode architecture, however, is difficult to scale for even higher sampling rates, because of the very short required sampling pulses with a 25% duty cycle. Therefore, we investigate a voltage mode architecture for the 1-to-4 ADeMUX that can use a 50% duty cycle clock and has therefore relaxed requirements for the clock generation and distribution. Furthermore, voltage mode T/Hs using a switched emitter follower (SEF) have been able to demonstrate comparable bandwidths of 60–70 GHz, if appropriate linearization techniques are applied [3], [4]. As shown in Fig. 1, they are ideally suited for time interleaving with their combination of ultra-high sampling rate and an input bandwidth that covers multiple Nyquist zones. This paper elaborates on a way of implementing four of these voltage mode T/Hs in a time interleaved ADeMUX, to reach a sampling rate of up to 4 x 50 GS/s = 200 GS/s in total.

II. Circuit Design

A block diagram with the topology of the voltage mode 1-to-4 ADeMUX and a chip microphotograph are shown in Fig. 2, detailed circuit diagrams of the quadrature clock path with 50% duty cycle and the analog core are depicted in Fig. 3 and Fig. 4, respectively.



(a) (b)

Fig. 2. (a) Block diagram of the 1-to-4 voltage mode analog demultiplexer. (b) Microphotograph of the die, wire-bonded to an RF evaluation board.

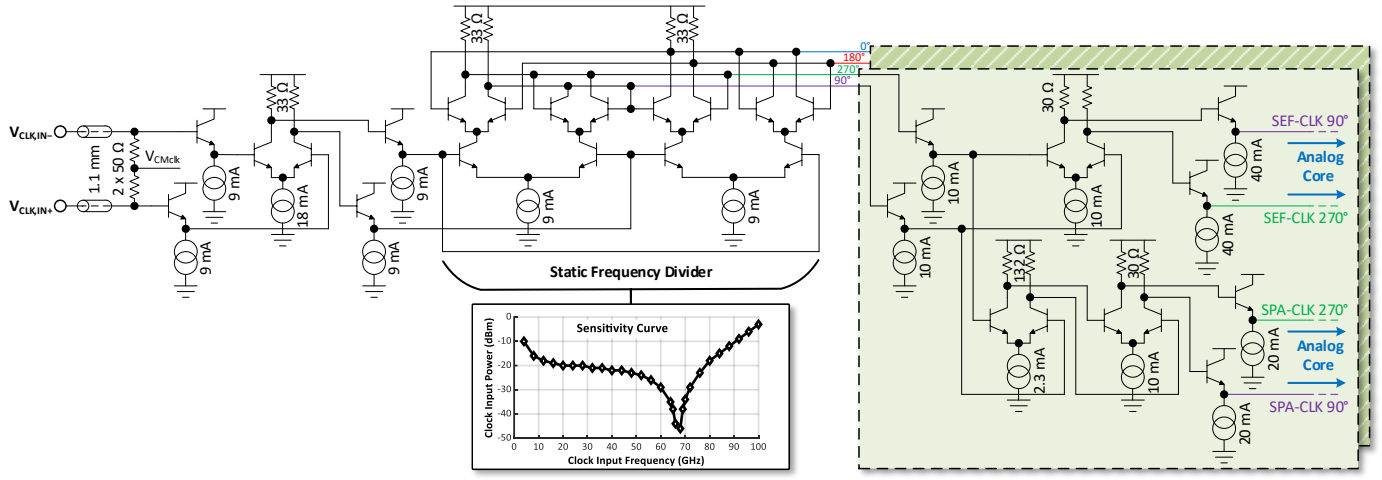


Fig. 3. Quadrature clock path of the voltage mode ADeMUX with 50% duty cycle, the inset shows the 67 GHz self-oscillation frequency of the static divider.

The circuit contains four T/H cores with a switched preamplifier (SPA), a SEF, and an emitter follower (EF) output buffer, as presented for the SEF-based single-channel T/H in greater detail in [3]. The EF output buffer Q_{32}/Q_{39} with series termination causes the output voltage to be half the value at the input of the circuit but guarantees linear broadband operation. Two T/H cores with opposite clock polarity share one EF input buffer Q_0/Q_7, decoupling them from the other pair. The input buffers have a joint base node, where the 50-Ω termination resistors, custom 1.1-mm long differential 100-Ω transmission lines, and the 50 µm x 65 µm large input wire-bond pads are placed. The T/H pairs with opposite clock polarity share not only a common input buffer, but also a common clock driver branch. It consists of a classic differential amplifier (DA) and an EF output buffer with a large tail current in the clock path for the SEF, and an additional delay DA for the SPA path. This delay ensures that the hold capacitor of the SEF is disconnected from its input node before the latter is switched to zero by the SPA. Both the clock branch for the SEF and for the SPA share a common EF input buffer. The quadrature phase relation is obtained by a static frequency divider in current mode logic, with a simulated input-related self-oscillation frequency of 67 GHz, as shown in Fig. 3. In front of the frequency divider, another DA stage with EF input and output buffers is placed, as well as another 1.1 mm long differential 100-Ω transmission line, termination resistors, and wire-bond pads. Bias voltages are generated on-chip from a single 4.85 V supply voltage. The current consumption is 720 mA, resulting in a DC power dissipation of 3.5 W, with 49% assigned to the clock path, 45% to the analog core, and 6% to biasing.

III. Experimental Results

The chip is wire-bonded onto the same RF module as the one in [2] for characterization. It consists of a 250 µm thick layer of ceramic-filled PTFE substrate Rogers3006, two 35 µm thick copper layers, and Au coating. The signal interfaces are 70-GHz GPPO connectors and SMP-Mini cables. The backside of the PCB is fixed on a 1 mm thick copper heatsink that is mounted onto a large Al heat spreader. The measurement setup is shown in Fig. 5. The highest frequency provided by the available signal generators is 70 GHz, which would correspond to a sampling rate of 4 x 35 GS/s = 140 GS/s, due to the static frequency divider on the ADeMUX chip. To reach sampling rates of up to 200 GS/s, we use a 20–100 GHz frequency doubler based on GaAs diodes. In this setup, the signal generator connected to the input of the module can provide the required input swing up to 42 GHz. When we use this signal generator for the clock, we can measure input signals with up to 57 GHz at 0.5 V_{pp} input swing.

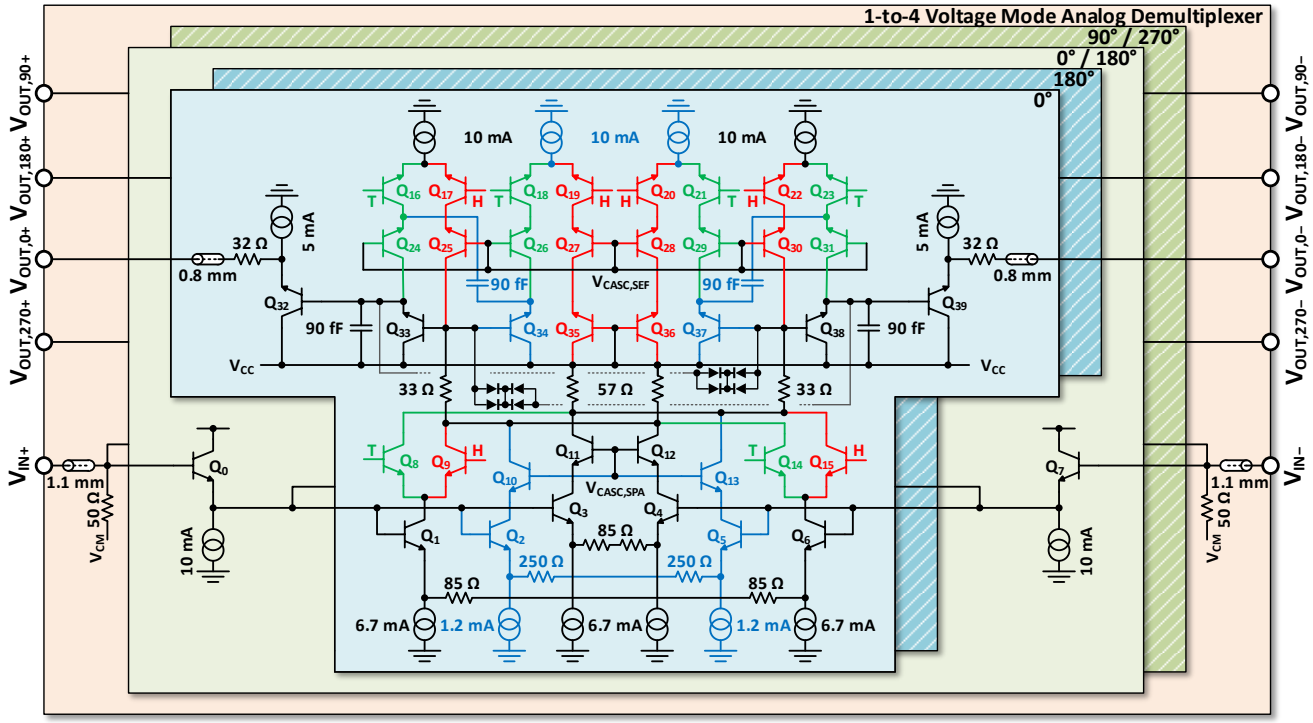


Fig. 4. Schematic of the analog core of the 1-to-4 analog demultiplexer. Track (**green**) and hold (**red**) branches are marked for the switched preamplifier (bottom) and the switched emitter follower (top) alongside their respective linearization branches (**blue**).

The signal level for the input of the ADeMUX module was first calibrated with the input cable and balun, then together with 2 x 20 mm long on-board transmission lines with cables connected on both ends, to build an interface with double the dimensions of the module's input. The attenuation of this reference line was measured and half of it was added to the targeted signal level, in addition to the input cable and balun losses. Fig. 6 shows the measured frequency response at 128 GS/s and at the maximum sampling rate of 200 GS/s that is allowed by the experimental setup, as well as the amplitude mismatch between the four output channels. At 128 GS/s, the input bandwidth is 50 GHz at 1 V_{pp} and more than 57 GHz at 0.5 V_{pp} input swing, clearly larger than the 32–40 GHz of state-of-the-art ADCs [1], [6]. At 200 GS/s, the worst attenuation is –9 dB within the measured frequency range of 42 GHz. In [7], an input bandwidth of 58 GHz was measured at 4 x 5 GS/s, which is only 10% of the targeted single-lane sampling rate for a 200 GS/s 1-to-4 ADeMUX and is therefore closer to the track mode bandwidth than to full 200 GS/s operation. However, the large jitter in our setup due to imperfect synchronization of the clock and data signal generators causes a high noise voltage, making it difficult to assess the dynamic performance, such as the spurious-free dynamic range (SFDR) and the total harmonic distortion (THD), without averaging. Fig. 7 shows the measured traces and an exemplary frequency spectrum obtained from a 128-point DFT in the hold phases of the signal. The SFDR of the circuit is 20–38 dBc with 1 V_{pp} input swing, as shown in Fig. 8, using 16 averaged traces. This suppresses noise contributors, but not deterministic non-linearities like harmonic distortions. The maximum measured SNR corresponds to the SNR of the reference path at the sampling frequency, its shape indicating 700 fs sampling jitter.

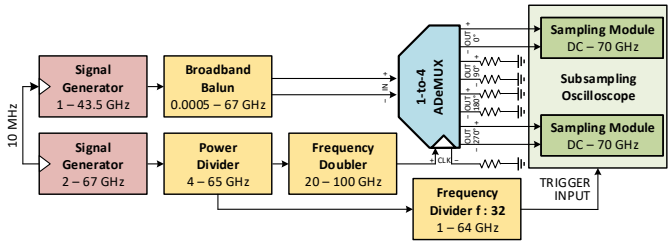


Fig. 5. Measurement setup for 200 GS/s maximum sampling rate. The signal generators are swapped to assess the performance above 40 GHz at 128 GS/s.

IV. Conclusion

Table I compares the voltage mode ADeMUX to the state-of-the-art. At 4 x 32 GS/s = 128 GS/s, the presented ADeMUX shows the highest input bandwidth above 64 GS/s of more than 50 GHz with an SFDR above 20 dBc, or 3 bit, up to 53 GHz. With this performance, 128-Gbaud pulse amplitude modulation (PAM) should be possible with multiple levels, as 256-Gbit/s PAM-4 eye diagrams were shown in [2] with lower ADeMUX bandwidth. When exploiting the full measurement capability, we can operate the device at the highest reported sampling rate of 4 x 50 GS/s = 200 GS/s, although the dynamic performance of the first device to achieve this sampling rate in [7] is considerably higher at the same sampling rate. Yet, 200-Gbaud on-off-keying (OOK) could be possible with this simpler quadrature clock path architecture that uses a 50% duty cycle, since the frequency divider is still working at 100 GHz input clock frequency. Hence, this time interleaving SiGe front end can contribute to coherent optical modules at 800 Gbit/s with the simplest or more than 1 Tbit/s gross data rate with multi-level I/Q modulation and dual polarization, using four CMOS ADCs with only 16–25 GHz bandwidth in a silicon receiver.

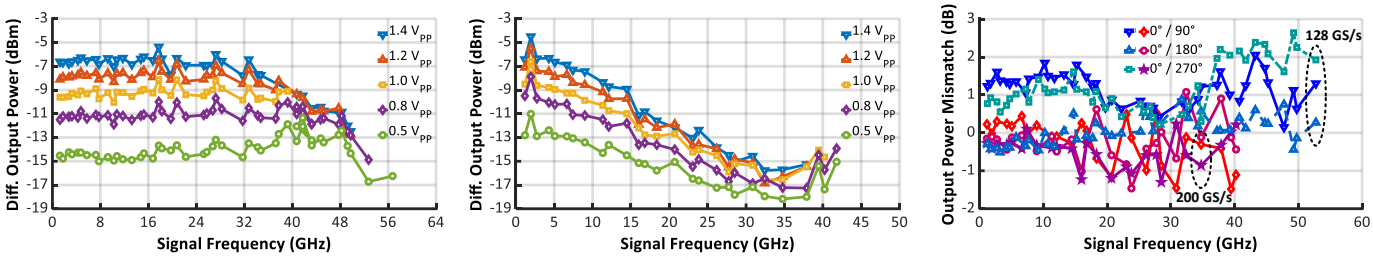


Fig. 6. Measured frequency response for different input voltage swings (a) at 128 GS/s and (b) at 200 GS/s, (c) amplitude mismatch between the output channels.

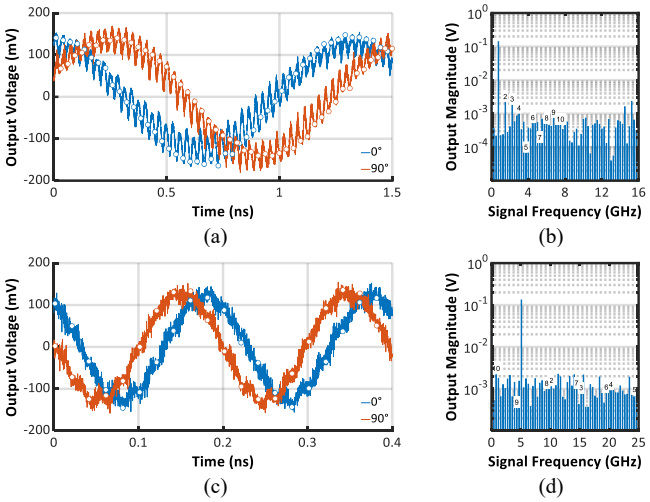


Fig. 7. Measurement with 1 V_{pp} input voltage swing. (a) Transient signal and (b) frequency spectrum with 32.75 GHz sampled at 128 GS/s, (c) transient signal and (d) frequency spectrum with 5.078 GHz sampled at 200 GS/s.

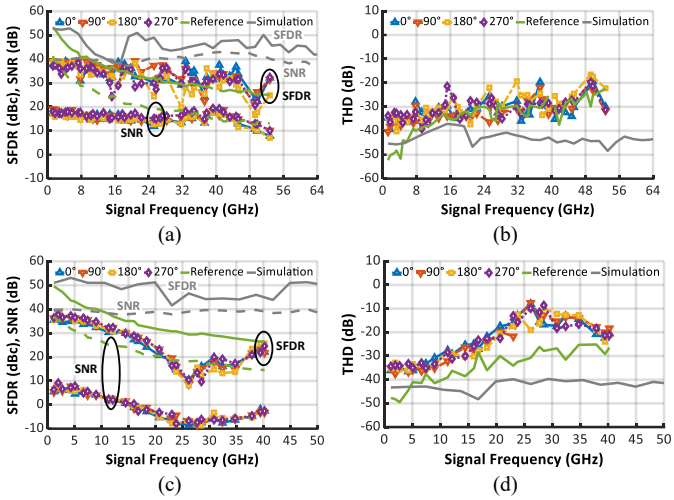


Fig. 8. Measurement with 1 V_{pp} input voltage swing, with (SFDR, THD) and without (SNR) averaging of 16 traces. (a) SFDR and SNR, (b) THD sampled at 128 GS/s; (c) SFDR and SNR, (d) THD sampled at 200 GS/s.

TABLE I. COMPARISON OF STATE-OF-THE-ART ANALOG SAMPLING FRONT ENDS AND ADCS.

Reference	[4]	[5]	[6] *)	[2]	[7]	**This Work**	
Technology	130 nm SiGe	130 nm SiGe	55 nm SiGe	90 nm SiGe	55 nm SiGe	**90 nm SiGe**	
f_T / f_{MAX}	300/500 GHz	300/450 GHz	330/370 GHz	300/480 GHz	320/370 GHz	**300/480 GHz**	
f_S (GS/s)	40	4 x 28 = 112	2 x 64 = 128	4 x 32 = 128	4 x 50 = 200	**4 x 32 = 128**	**4 x 50 = 200**
f_{3dB}	70 GHz @ track mode	–	32 GHz	36 GHz (f_{6dB} 50 GHz)	58 GHz @ 4 x 5 GS/s	**50 GHz @ 1 V_{pp} >57 GHz @ 0.5 V_{pp}**	**15 GHz @ 1 V_{pp} 20 GHz @ 0.5 V_{pp} (f_{6dB} 30 to >42 GHz)**
SFDR	29–55 dBc	35–49 dBc	30–38 dBc	25–40 dBc	25–48 dBc	**20–38 dBc @ 1 V_{pp}**	**10–37 dBc @ 1 V_{pp}**
Freq. Range	1–19 GHz	1–43 GHz	1–32 GHz	1–50 GHz	1–70 GHz	**1–53 GHz**	**1–41 GHz**
DC Power	0.44 W	3.3 W	1.3 W	2.6–3.6 W	0.64 W	**3.5 W**	

*) Full 5-bit ADC-DAC combination.

ACKNOWLEDGMENT

We thank Infineon Technologies for the manufacturing and donation of the dies, as well as Peter Klose of Nokia Bell Labs and Benedikt Heislbetz for assembling the RF modules.

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