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WS-01 - SiGe BiCMOS Integrated circuits for millimeter-wave applications: 5G , automotive radars, imaging,... - at

2019 European Microwave Conference (EuMC 2019), Paris, France
Sept 29 - Oct 9, 2019.

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SiGe BiCMOS Integrated circuits for millimeter-wave applications: 5G, automotive radars, imaging, ...

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D/A and A/D Conversion Key ICs for Broadband Communications

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M. Collisi[3], M. Möller[3]
H. Hettrich[4], A. Bielik[4], R. Schmid[4]
K. Schuh[5], F. Buchali[5]

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[3]University of Saarland, Saabrücken, Germany (USAAR)
[4]Micram GmbH, Bochum, Germany (MICRAM)
[5]Nokia Bell Labs, Stuttgart, Germany (NOKIA)

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1. Why SiGe-HBTs for ADC/DAC Front-Ends ?

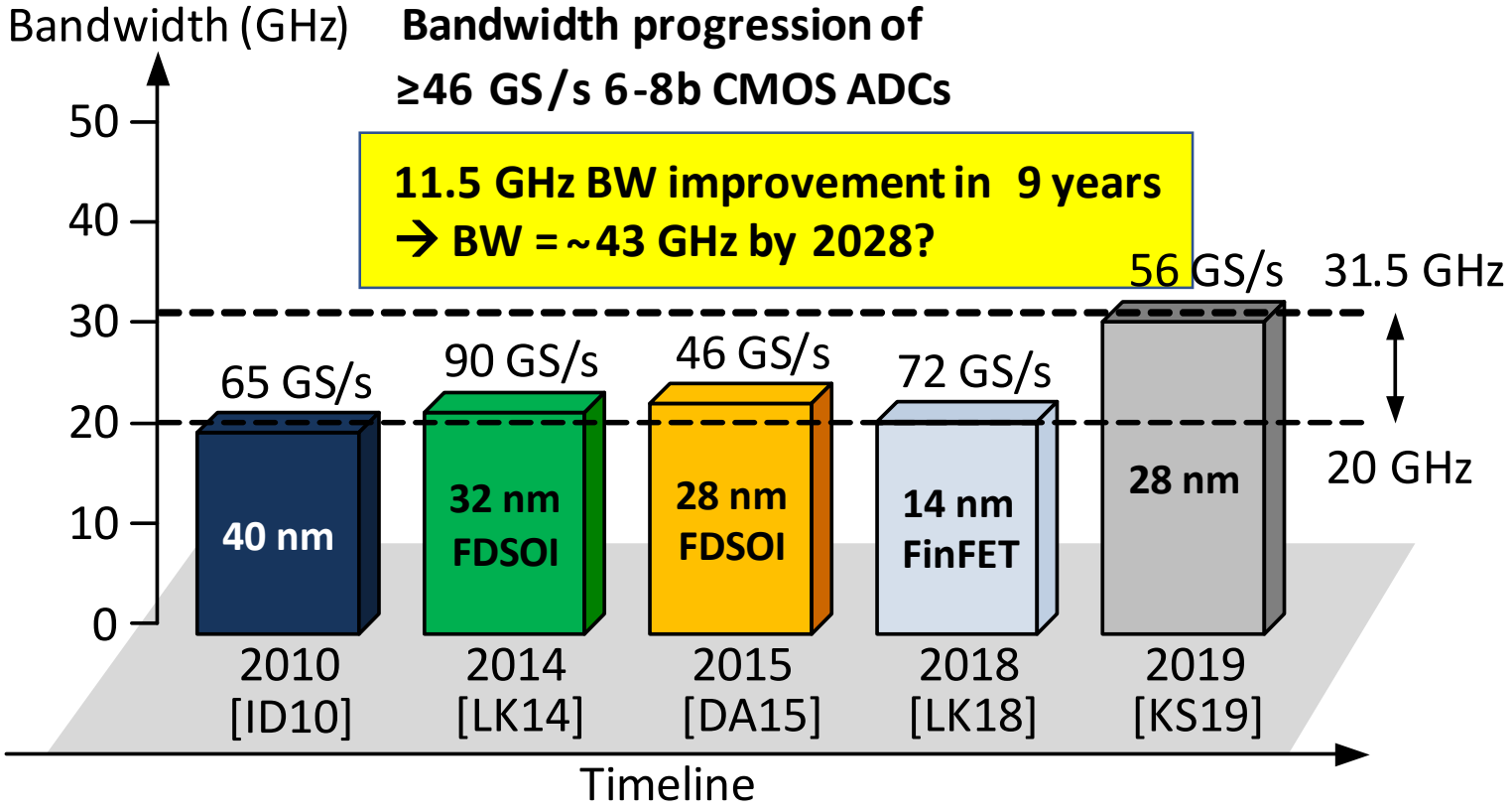
- **Application Demands for Broadband Converters**
  - **Optical data links**
    single-channel bandwidth demand is increasing further to increase data throughput with constant number of optical carriers (cost!) Current drivers:
    - intra- and inter-data-center connects
    - Connection of data centers to the metro networks
  - **mm-Wave and THz wireless networking**
    Single-channel bandwidth demand is also increasing
- **Circuit and Technology Solutions**
  - **ADCs and DACs in leading-edge CMOS technologies**
    (synchronous time-interleaved architectures inside)
    - have shown an considerable performance increase:
      conversion rates now up to ~120 GS/s in 16nm FinFET [T. Drenski, J.C. Rasmussen, OFC 2018]
    - **but analog input/output bandwidth stays limited to 20…30 GHz** [see next slide]

→ A solution is needed to increase the input/output bandwidth of converters

- **Analog Front-End Interleavers**
- **Ultra-High-Bandwidth Single-Core Converters**

in leading-edge maximum f_T/fmax SiGe-HBT technologies

1. Conversion Rates and Bandwidth of CMOS Converters



[ID10] I. Dedic, "56Gs/s ADC : Enabling 100GbE," 2010 Conference on Optical Fiber Communication (OFC), San Diego, CA, 2010, pp. 1-3.

[LK14] L. Kull et al., "22.1 A 90GS/s 8b 667mW 64× interleaved SAR ADC in 32nm digital SOI CMOS," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, 2014, pp. 378-379.

[DA15] Y. Duan and E. Alon, "A 6b 46GS/s ADC with >23GHz BW and sparkle-code error correction," 2015 Symposium on VLSI Circuits (VLSI Circuits), Kyoto, 2015, pp. C162-C163.

[LK18] L. Kull et al., "A 24–72-GS/s 8-b Time-Interleaved SAR ADC With 2.0–3.3-pJ/Conversion and >30 dB SNDR at Nyquist in 14-nm CMOS FinFET," in IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3508-3516, Dec. 2018.

[KS19] K. Sun, G. Wang, Q. Zhang, S. Elahmadi and P. Gui, "A 56-GS/s 8-bit Time-Interleaved ADC With ENOB and BW Enhancement Techniques in 28-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 54, no. 3, pp. 821-833, March 2019.

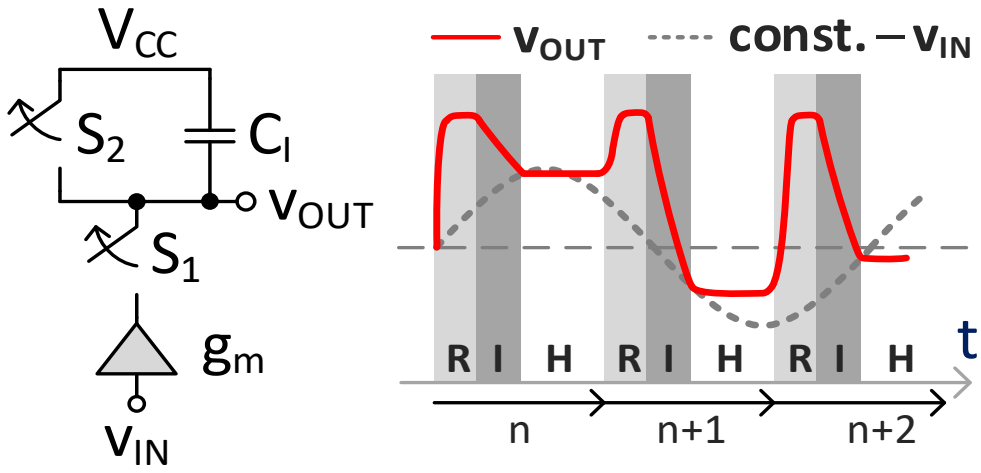
Outline - Approaches to More ADC/DAC-Bandwidth

1. Why SiGe-HBTs for ADC/DAC Front-Ends ?
2. **A/D Conversion: Time-Interleaving Analog Front-Ends**
   1. Synchronous Time Interleaving (STI) 1:4 AFE — USTUTT
   2. Asynchronous Time Interleaving (ATI) 1:4 AFE — URM1
3. **D/A Conversion: Time-Interleaving & Single-Core Front Ends**
   1. Analog Multiplexer (AMUX) 2:1 AFE — USAAR
   2. Ultra-High-Speed Single-Core DAC — MICRAM
4. **A/D and D/A Application Experiments** — NOKIA
5. **Conclusion**

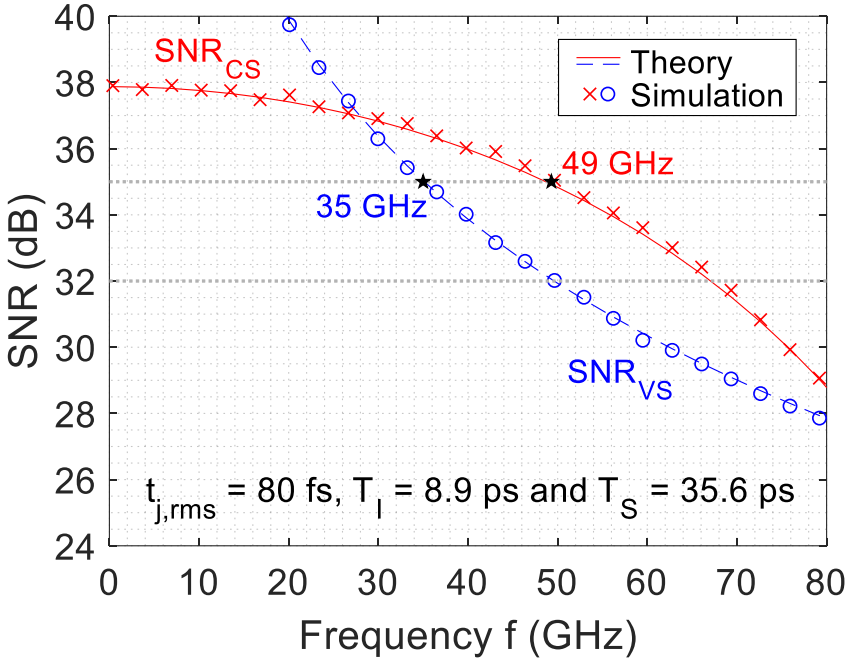
ATI: Asynchronous Time Interleaving
STI: Synchronous Time Interleaving
AFE: Analog Front End

ADC: Analog-to-Digital Conversion
DAC: Digital-to-Analog Conversion
AMUX: Analog Multiplexer

2.1 STI 1:4 AFE for ADC Introduction: Charge-Sampling



R = Reset, I = Integration, H = Hold



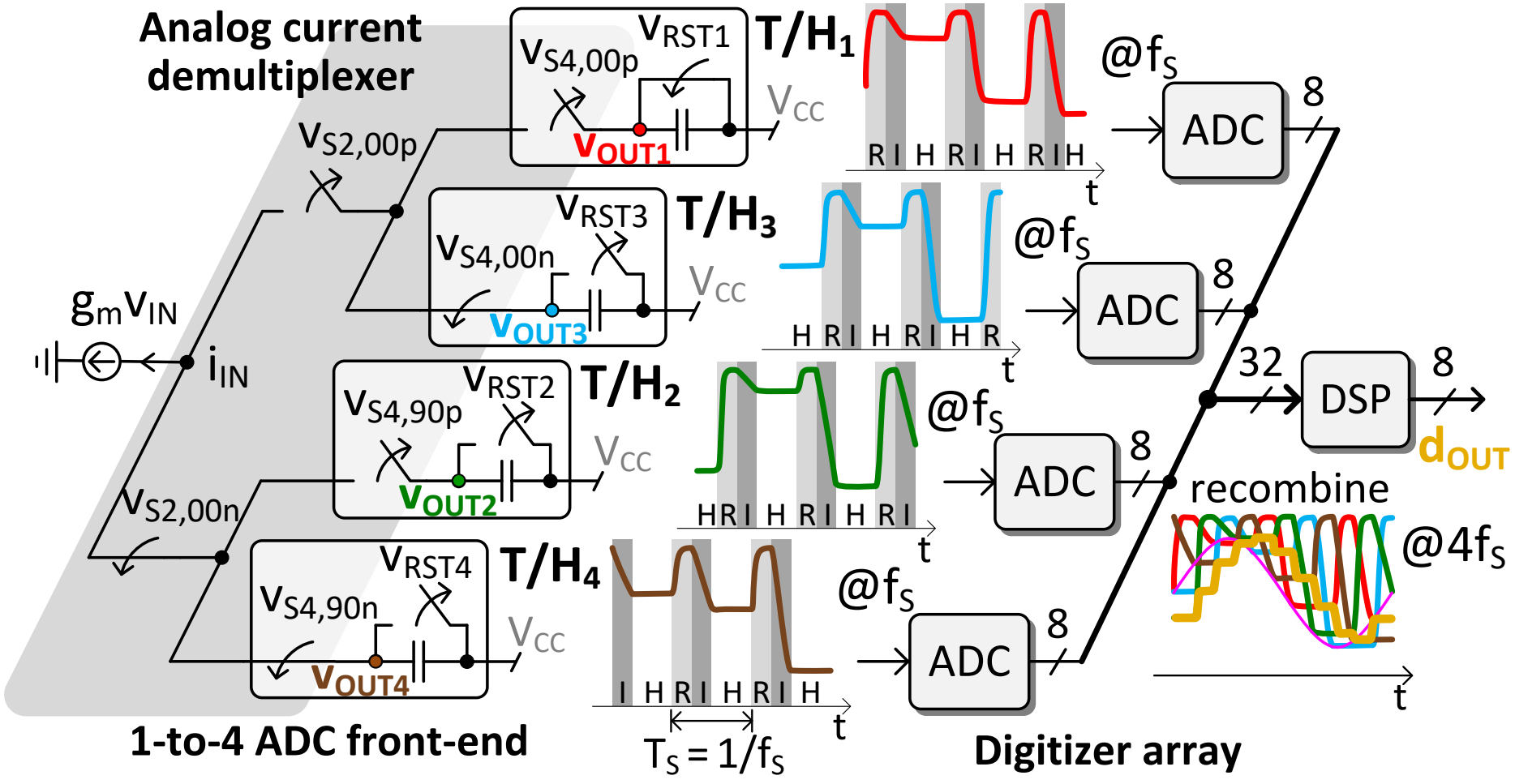
$$SNR_{CS} = \left(\frac{\sqrt{1 - \cos(2\pi f T_I)}}{2\pi f t_{j,rms}} \right)^2$$

$t_{j,rms}$ … root mean square (rms) sampling clock jitter
T_I … mean integration period

Charge-Sampling enables up to 3 dB SNR improvement for $f > \frac{1}{4T_I}$ for the same rms clk jitter

X.-Q. Du, M. Grözing, A. Uhl, S. Park, F. Buchali, K. Schuh, and M. Berroth, "A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019),* Boston, MA, USA, 2019.

2.1 STI 1:4 AFE for ADC: ADeMUX Operation Principle



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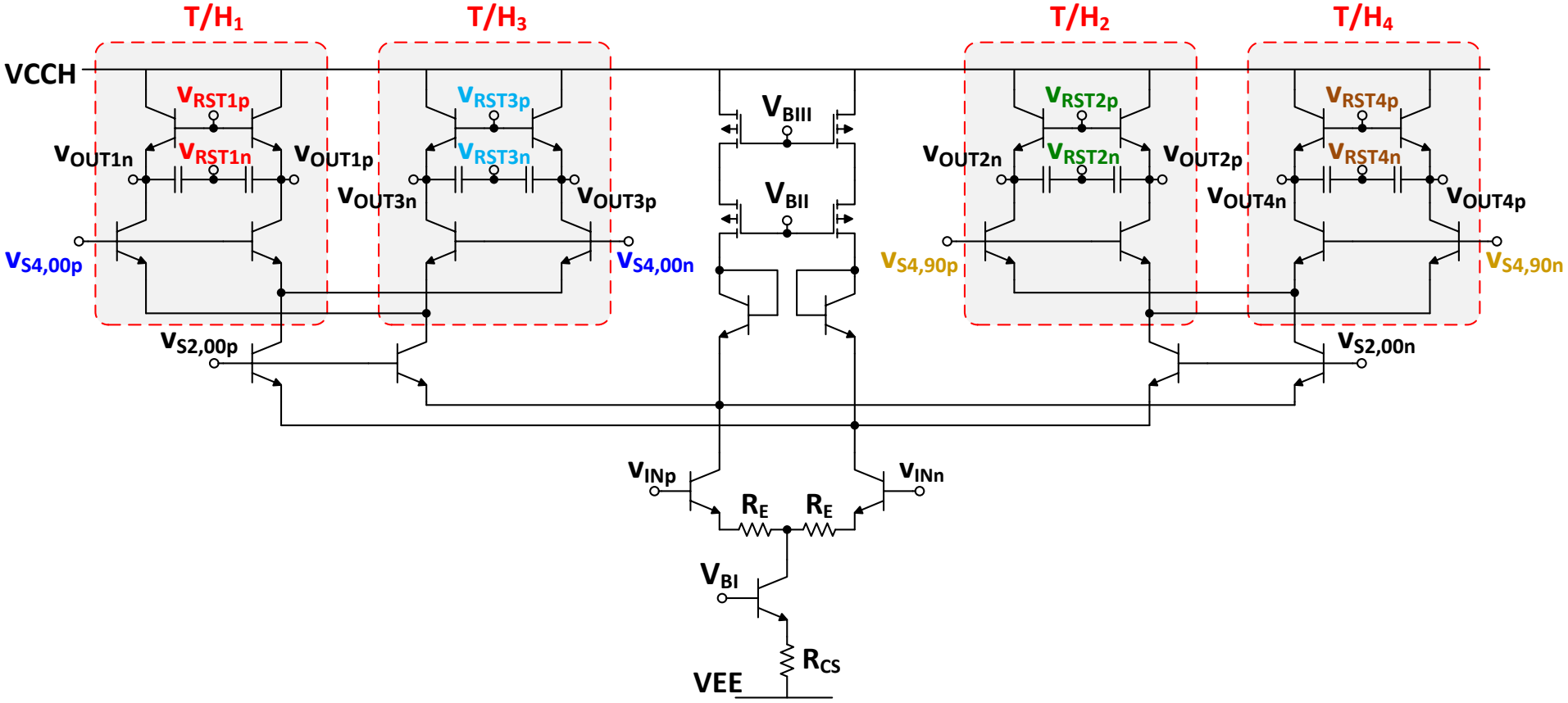
2.1 STI 1:4 AFE for ADC: ADeMUX Core Schematic



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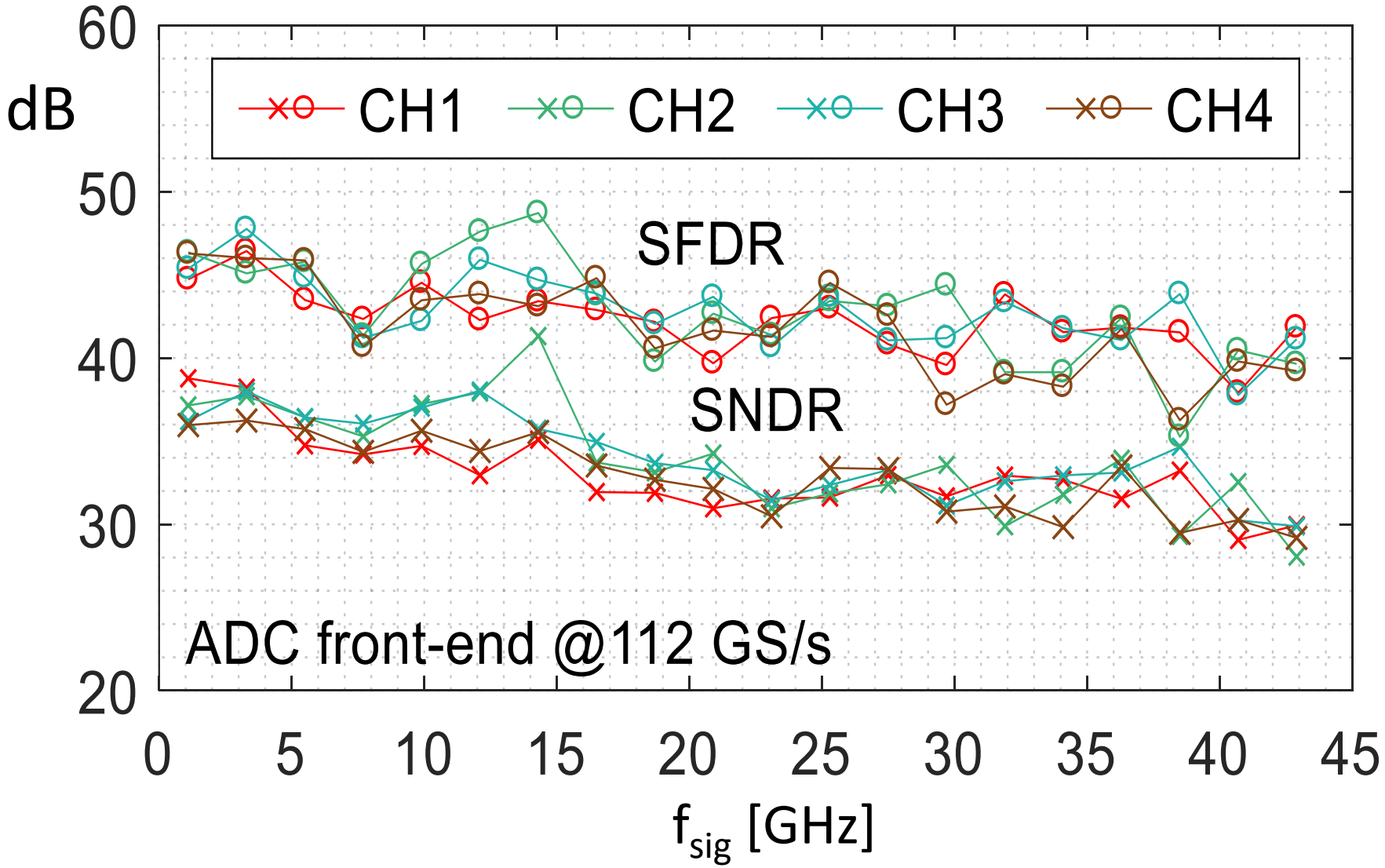
2.1 STI 1:4 AFE for ADC: Measurement Results



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2.1 STI 1:4 AFE for ADC: Summary

Time-interleaved samplers enabling ≥100 Gbaud PAM-4 reception

Parameter	This work	DSO [1]	DSO [2]
Sample rate (GS/s)	112 4x28	160	256 4x64
Frequency range (GHz)	DC–50	DC–63	DC–110
Technology	SiGe BiCMOS f_T = 300 GHz	InP	InP f_T = 600-700 GHz*
PAM-4 Baudrates	100 Gbaud 40 km SMF [3]	107 Gbaud 10 km SMF [4]	160 Gbaud 10 km SMF [5]

[1] Data sheet: https://prc.keysight.com/Content/PDF_Files/5991-3868EN.pdf
[2] Data sheet: https://literature.cdn.keysight.com/litweb/pdf/5992-3132EN.pdf
[3] F. Buchali *et al.*, "A SiGe HBT BiCMOS 1-to-4 ADC Frontend Supporting 100 GBaud PAM4 Reception at 14 GHz Digitizer Bandwidth," *OFC 2019,* Paper Th4A7.
[4] S. Kanazawa *et al.*, "Transmission of 214-Gbit/s 4-PAM signal using an ultra-broadband lumped-electrode EADFB laser module," *OFC 2016*, Paper Th5B.3.
[5] H. Yamazaki *et al.*, "160-GBd (320-Gb/s) PAM4 Transmission Using 97-GHz Bandwidth Analog Multiplexer," *IEEE Photonics Technology Letters*, vol. 30, no. 20, pp. 1749-1751, Oct.15, 2018.
*https://www.youtube.com/watch?v=DXYje2B04xE

First SiGe BiCMOS sampler for 100 Gbaud PAM-4 reception demonstrated

X.-Q. Du, M. Grözing, A. Uhl, S. Park, F. Buchali, K. Schuh, and M. Berroth, "A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019),* Boston, MA, USA, 2019.

2.2 2:1 ATI AFE for ADC: Introduction to ATI Principle

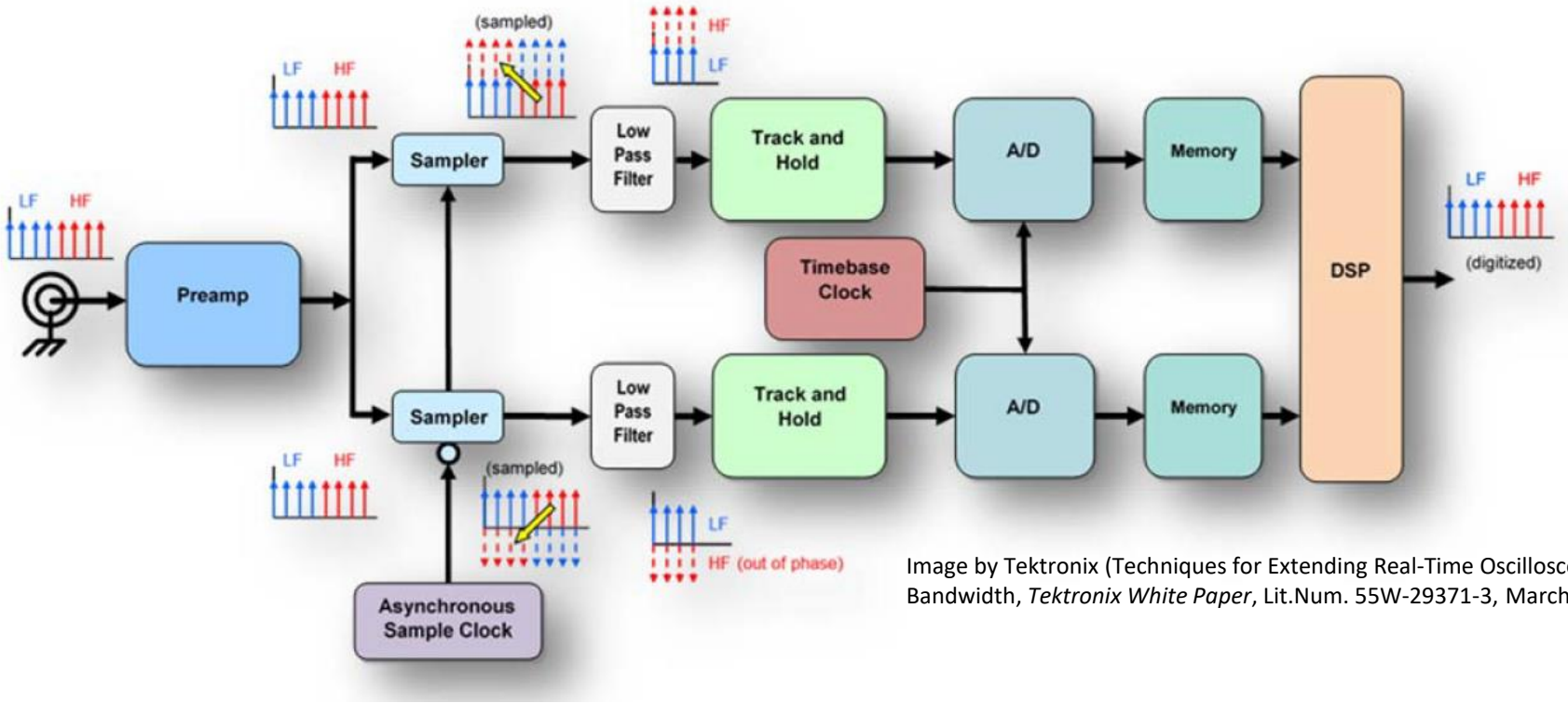


Image by Tektronix (Techniques for Extending Real-Time Oscilloscope Bandwidth, *Tektronix White Paper*, Lit.Num. 55W-29371-3, March 2015)

- Asynchronous Time-Interleaving (ATI)
  - Proposed by Tektronix and already used for 70GHz / 200GSps oscilloscopes
  - An analog interface pre-processes the signal alleviating the specifications for THAs and ADCs (required analog bandwidth is reduced)
  - Clocks in analog interface and sampling/digitizing can be asynchronous

2.2 2:1 ATI AFE for ADC: ATI Principle

Input signal

Sampling & Filtering (ATI AFE)

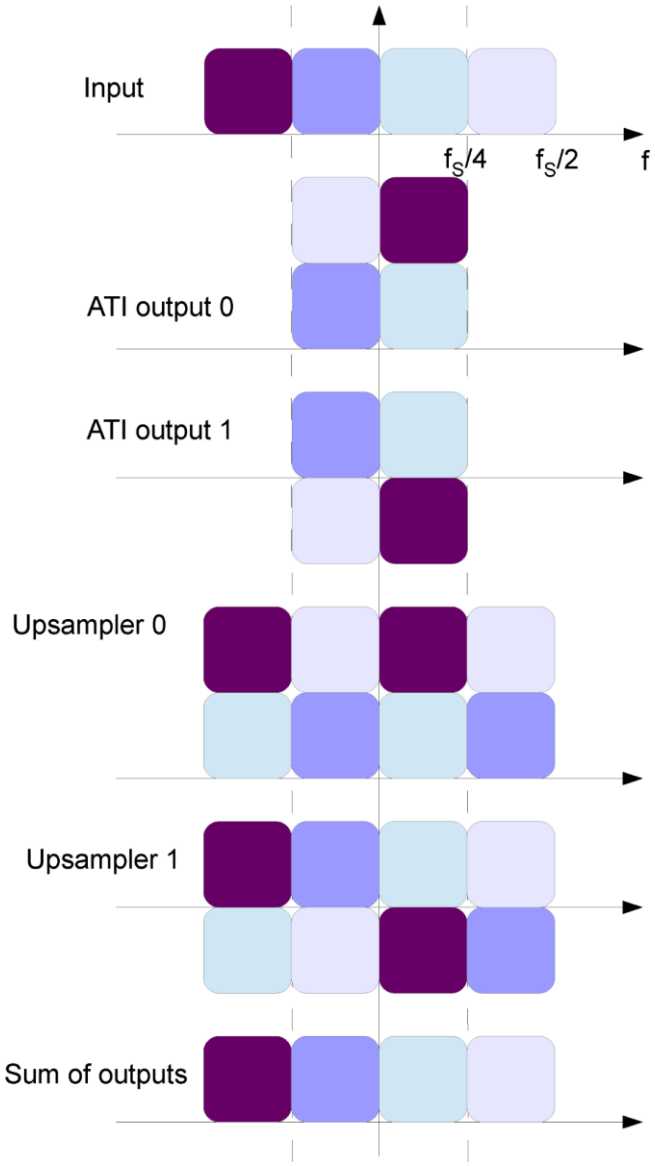
sampling with appropriate clock phases and lowpass filtering

Time-Interleaved ADCs

required analog bandwidth is fs/4; upsampling is implicit in recombination of outputs

Recombination of TI-ADC outputs

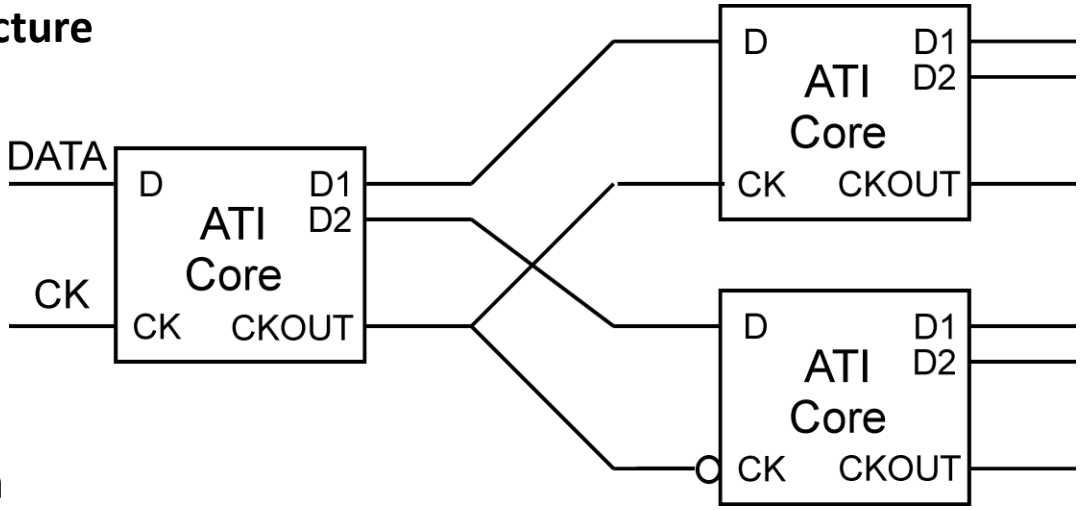
spectral components with opposite sign are cancelled



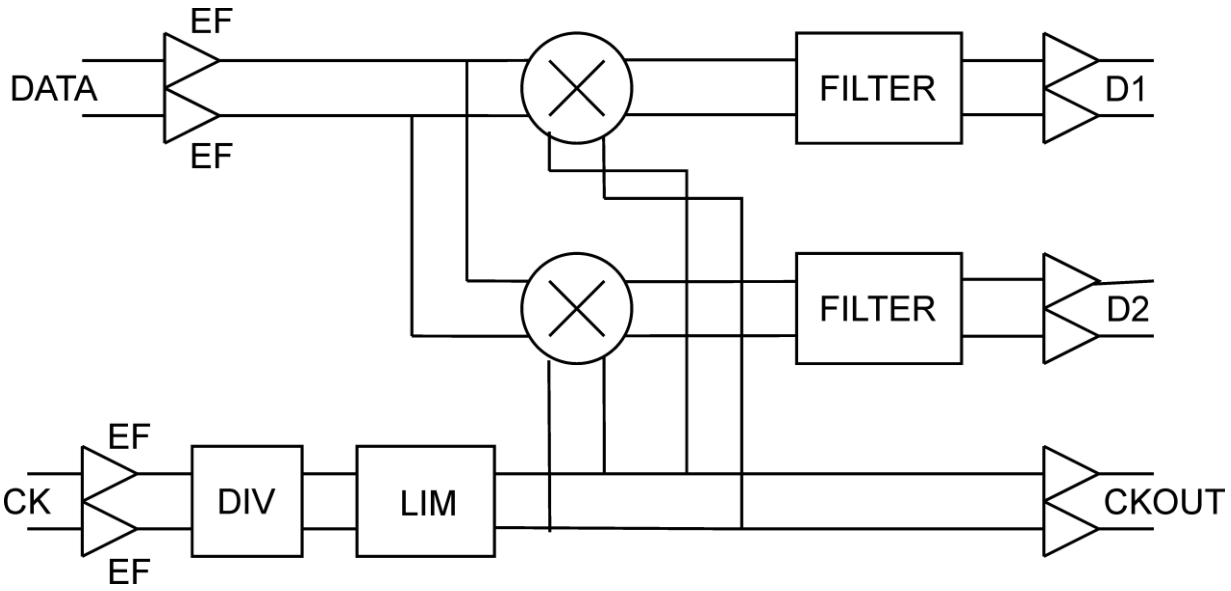
2.2 ATI AFE for ADC: Pulseless ATI Block Diagram

Hierarchical and Modular ATI Structure

The 2-channel ATI Core is a modular block that can be cascaded to obtain higher-order interleaving

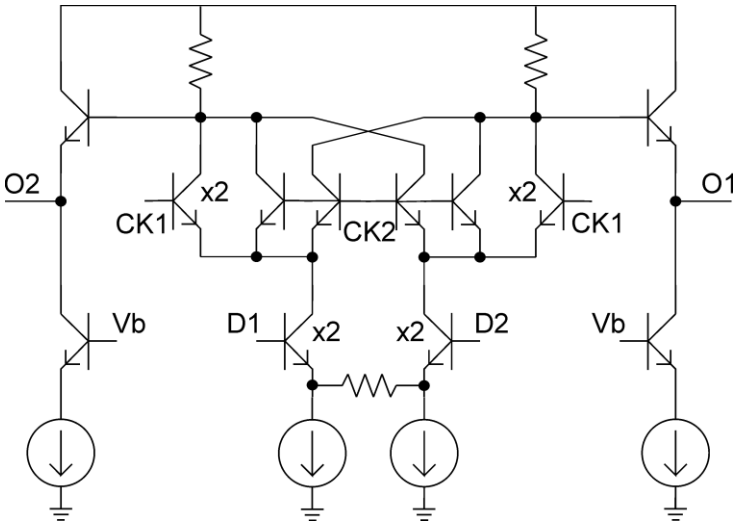


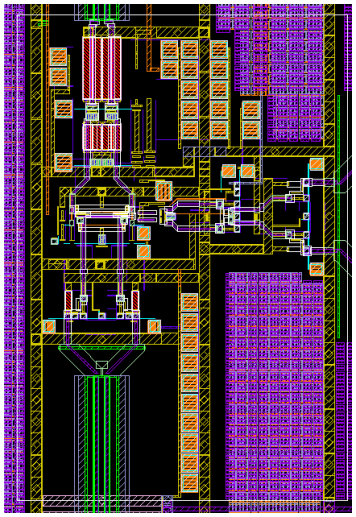
Single ATI Core Block Diagram

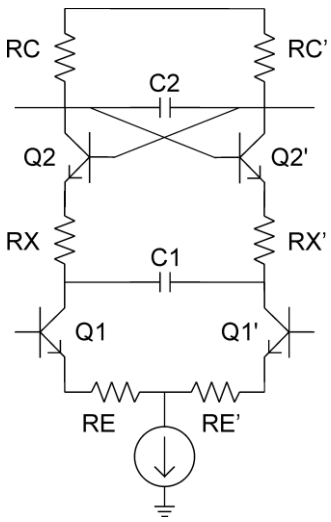


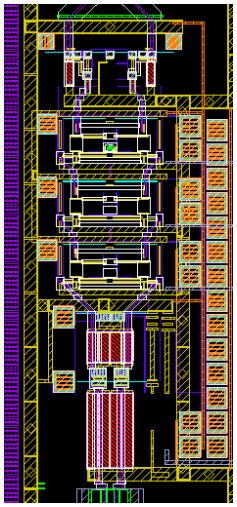
Pulseless ATI approach: the sampler (multiplication by pulses) is substituted by a mixer (multiplication by 1 and 0): 50% duty cycle of clock is required

2.2 ATI AFE for ADC: Building Blocks









Mixer block

DC Gain	0.1 dB
Output Bandwidth	22.8 GHz
HD3	-46.1 dB

Input/output buffer chain

DC Gain	-0.6 dB
3dB Bandwidth	46.5 GHz
HD3	-48.6 dB

Low pass filter

DC Gain	-0.6 dB
Peak	0.83 dB
3dB Bandwidth	11.2 GHz
Gain at 20 GHz	-32 dB
HD3	-42 dB
rms Input Noise	1.65 mV

Frequency divider (input: 40GHz sine)

Peak-peak Output Voltage	355 mV
Duty Cycle	49.95 %

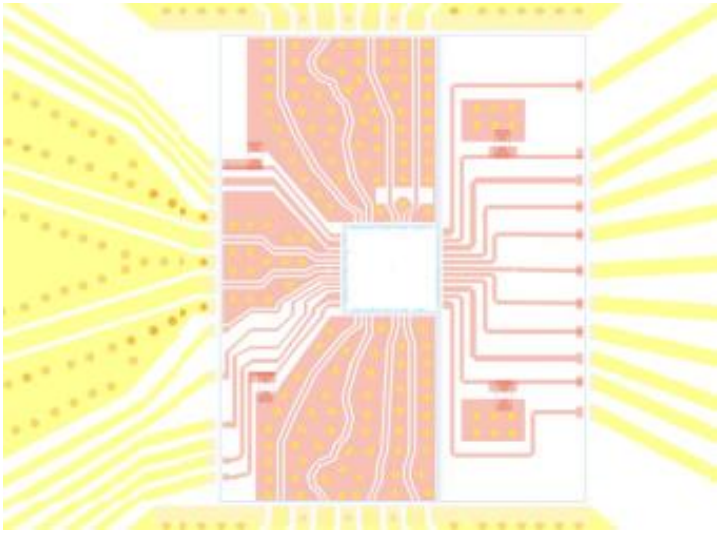
2.2 ATI AFE for ADC: ATI Test Chip

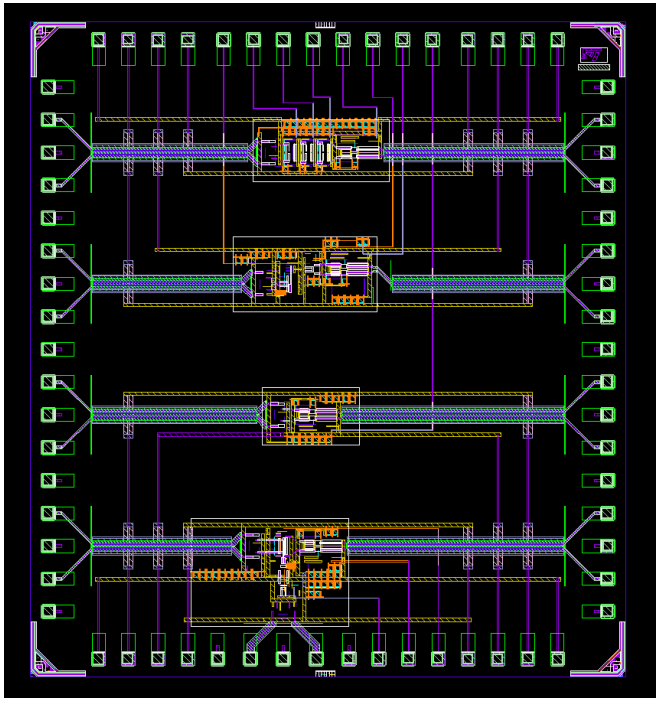
Test chip for 40 GS/s 2-channel ATI blocks designed (frequency divider, mixer, lowpass filter, output buffer)

Target:

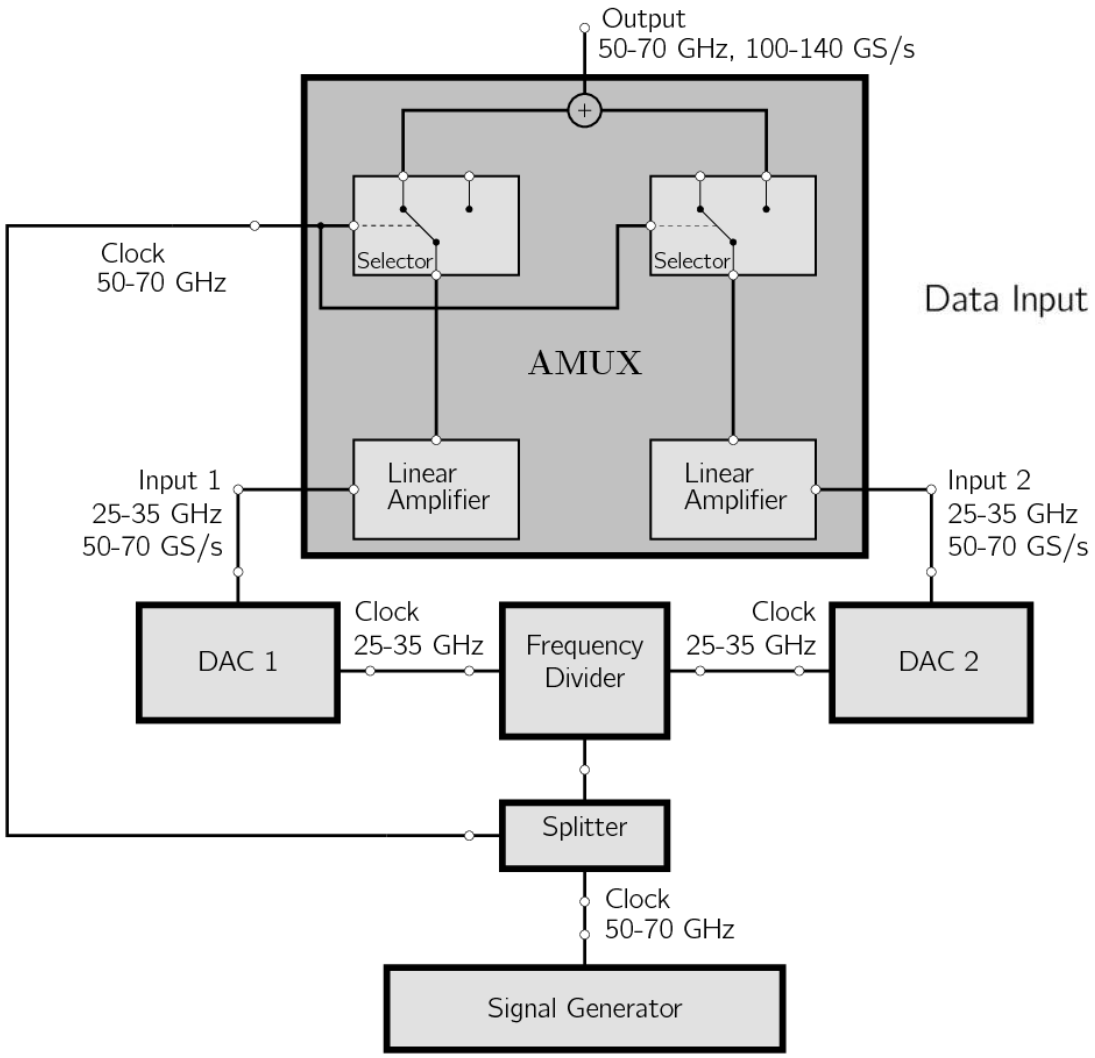
≥ 40 GS/s ≥ 20 GHz AFE 4-channel ATI output

4 commercial ADCs, i.e. AD9212 10-GSps 12-bit

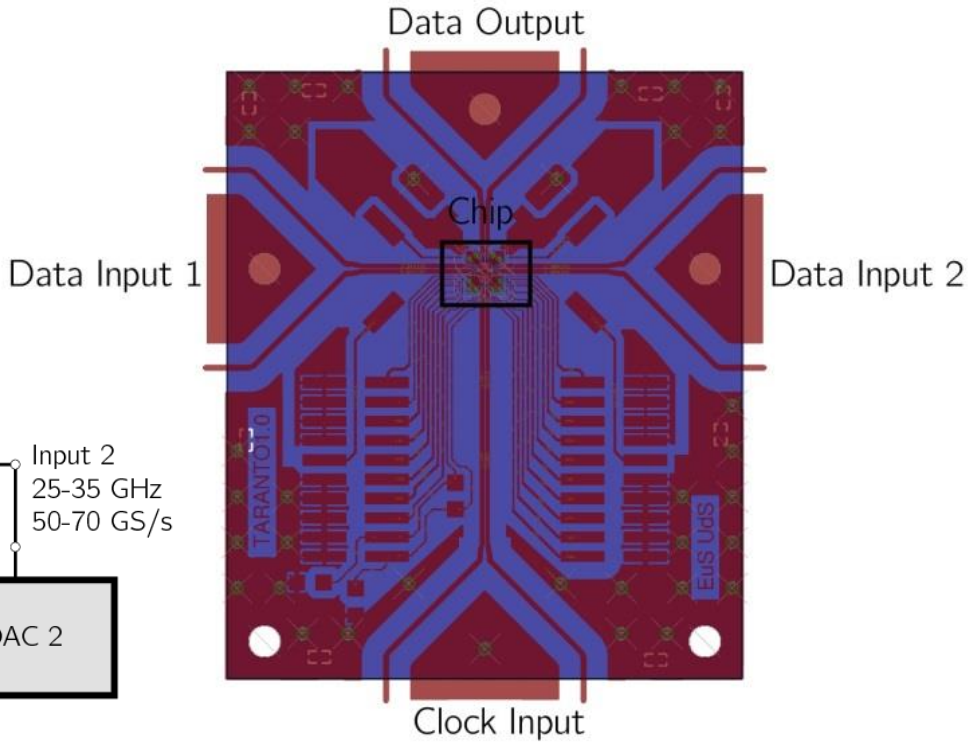




3.1 AMUX 2:1 AFE for DAC: Operation Principle



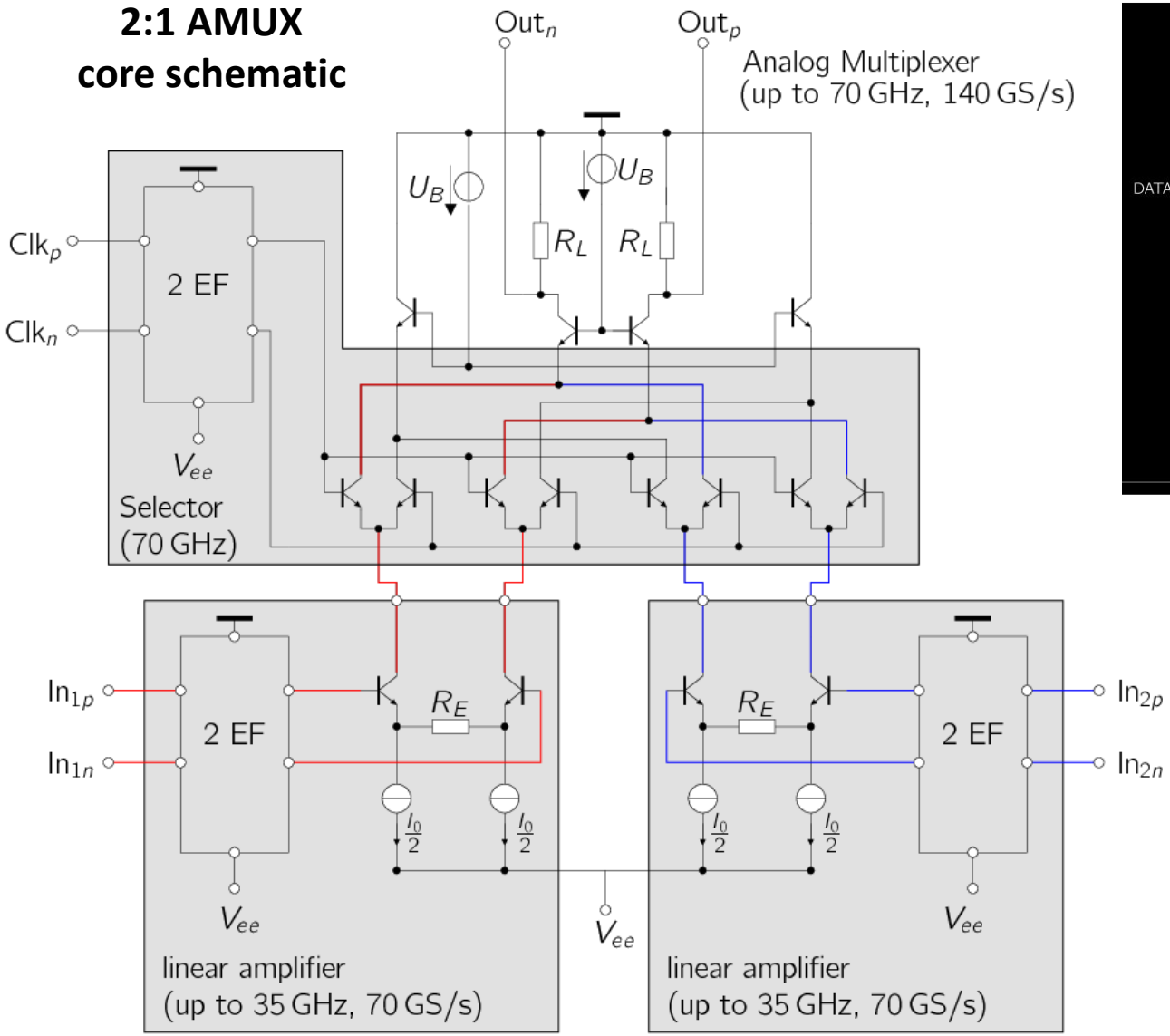
2:1 AMUX block diagram

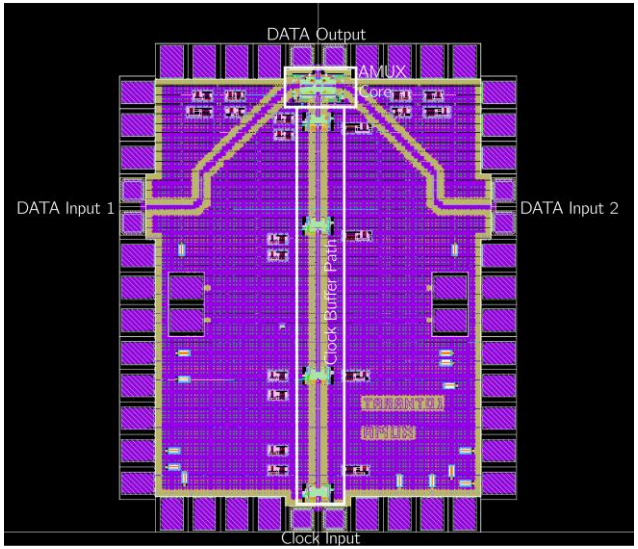


2:1 AMUX RF substrate layout

3.1 AMUX 2:1 AFE for DAC: Core Schematic

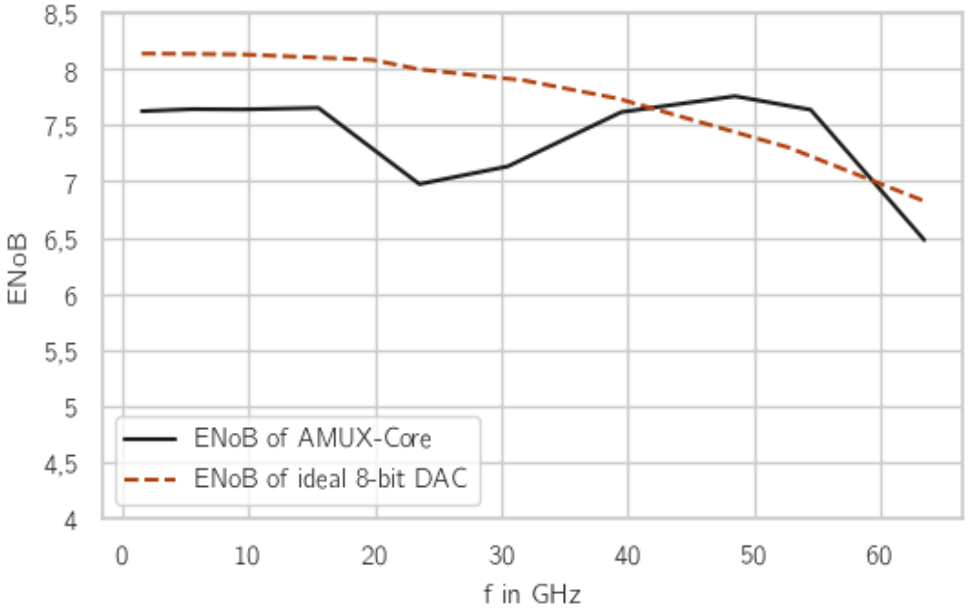
2:1 AMUX core schematic





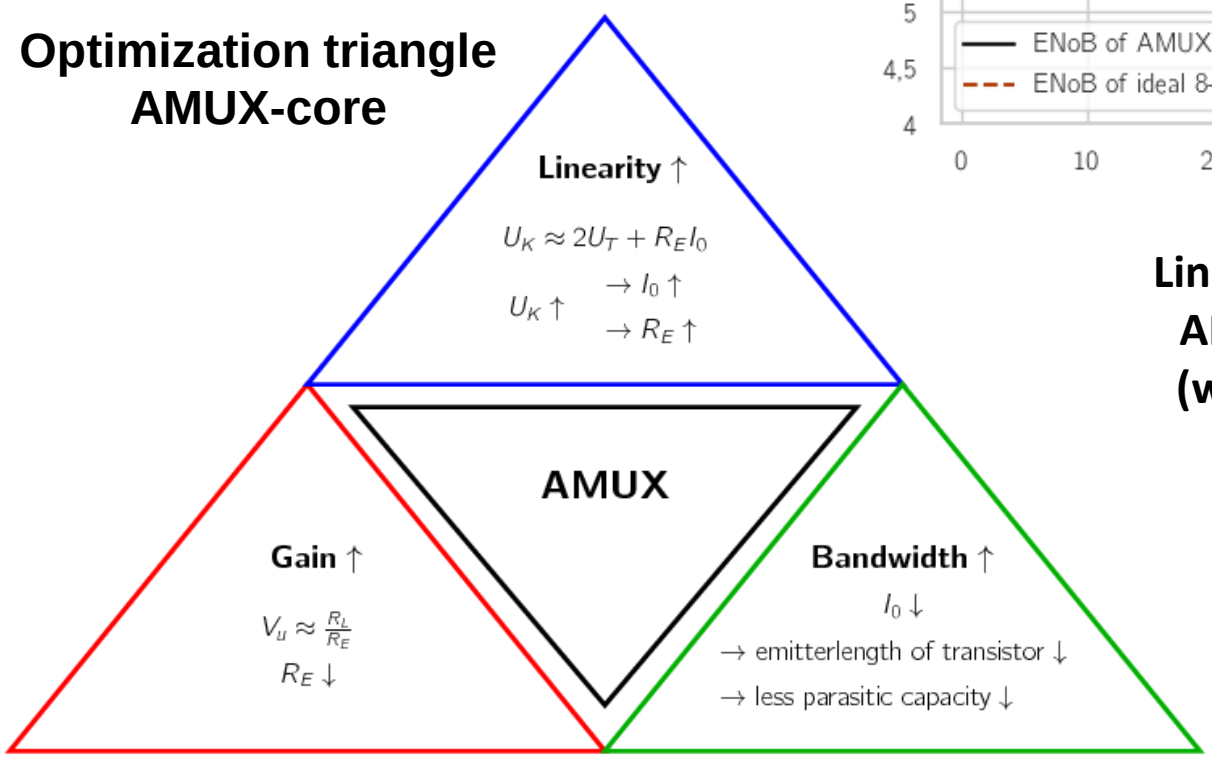
Layout of 2:1 AMUX IC
Die size: 1500 x 1300 µm²

3.1 AMUX 2:1 AFE for DAC: Dimensioning & Linearity



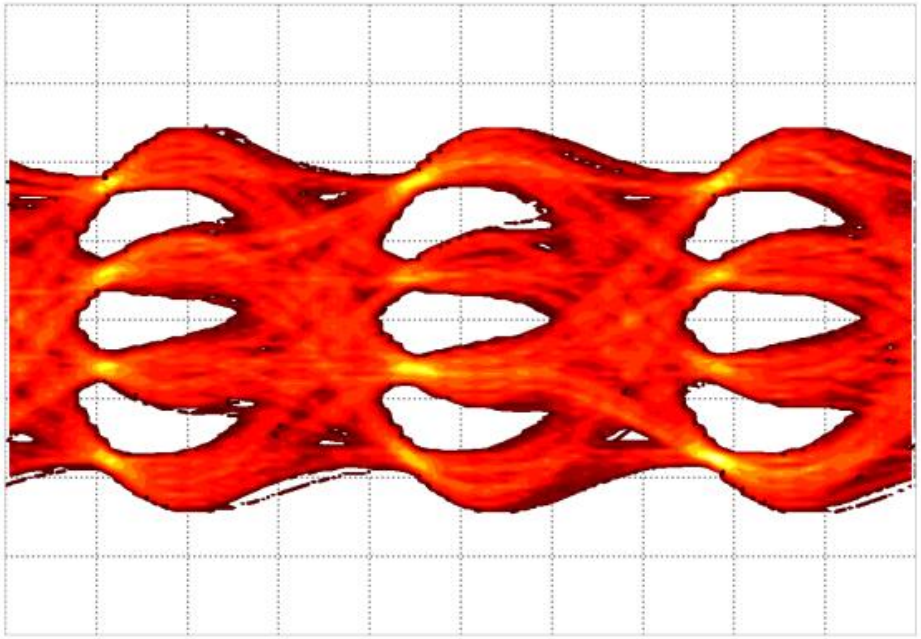
Linearity simulation result AMUX-core at 128 GS/s (without layout extract)

Optimization triangle AMUX-core

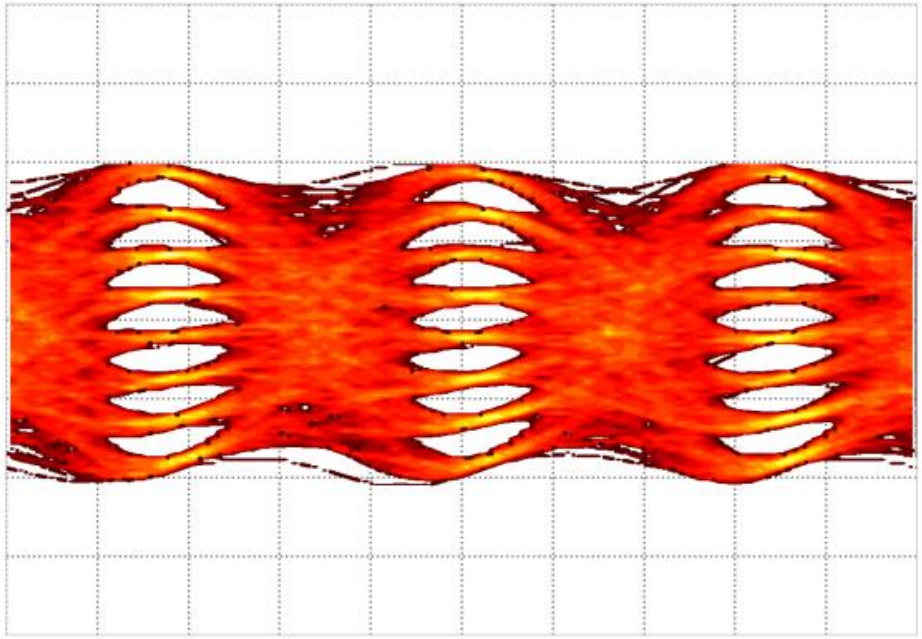


3.1 AMUX 2:1 AFE for DAC: Simulated Eye Diagrams

Simulated eye diagrams (with layout extract)



PAM-4 (128 GS/s, 200mV/div)



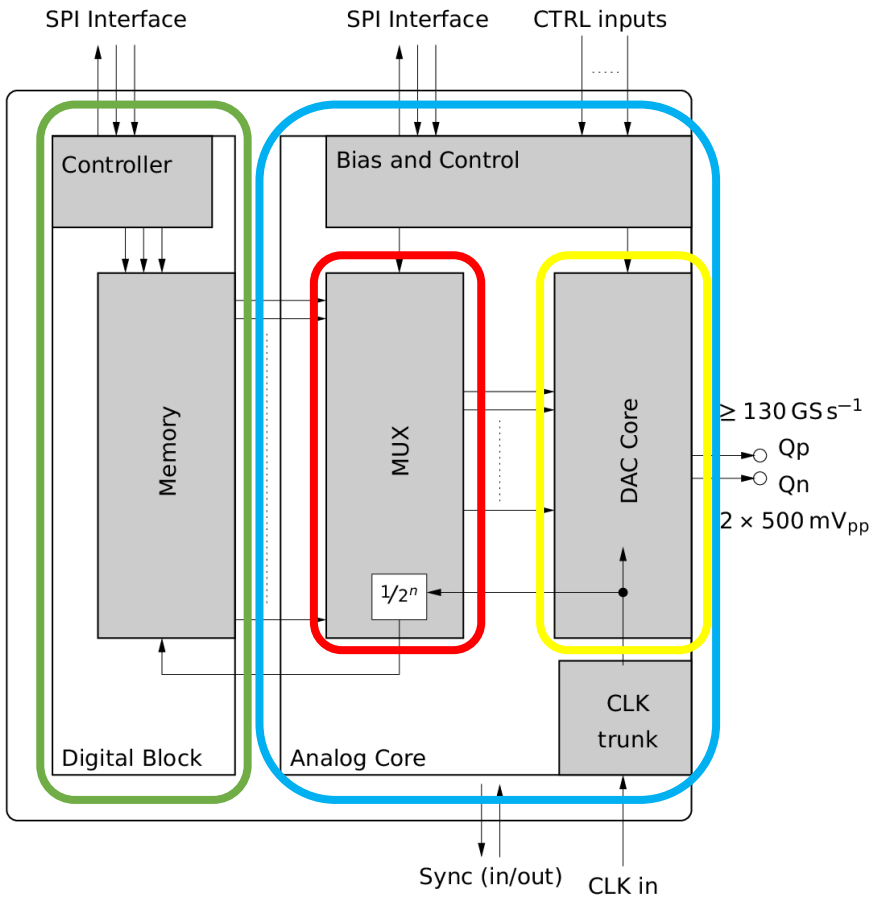
PAM-8 (100 GS/s, 200mV/div)

3.1 AMUX 2:1 AFE for DAC: Summary

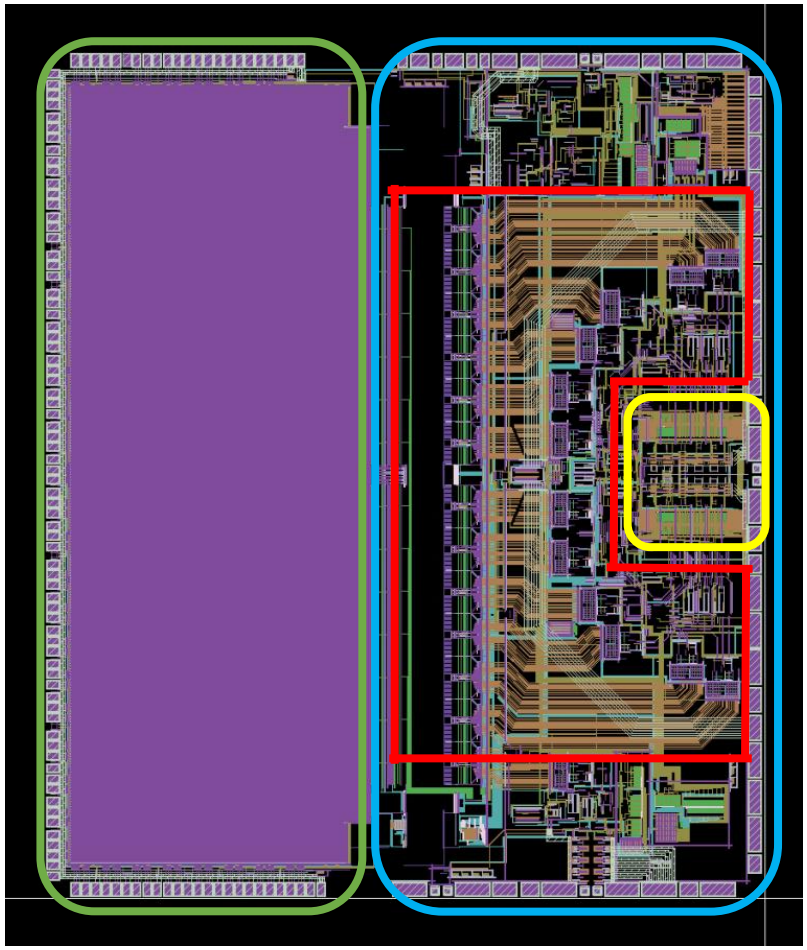
Parameter	Target Spec	Simulation/implemented at Tapeout
Sampling Rate SR=1/T	**≥ 100GS/s up to 128 GS/s**	**≥ 128GS/s**
ENoB	**≥ 6** within 1st Nyquist band	**> 6.5** within 1st Nyquist band (without layout extract) **> 7 up to 55 GHz** (without layout extract)
Gain	**V_u ≥ 1** (voltage gain)	**V_u = 0.8** (voltage gain)
Full Scale Swing	**1 Vpp differential** (500mVpp single-ended)	**800mVpp differential** (400mVpp single-ended)
Bandwidth	**> 50 GHz** (70 GHz targeted)	**> 70 GHz** (without substrate, connectors, …)

3.2 Single Core DAC: Block Schematic & Layout

DAC Simplified Block Diagram

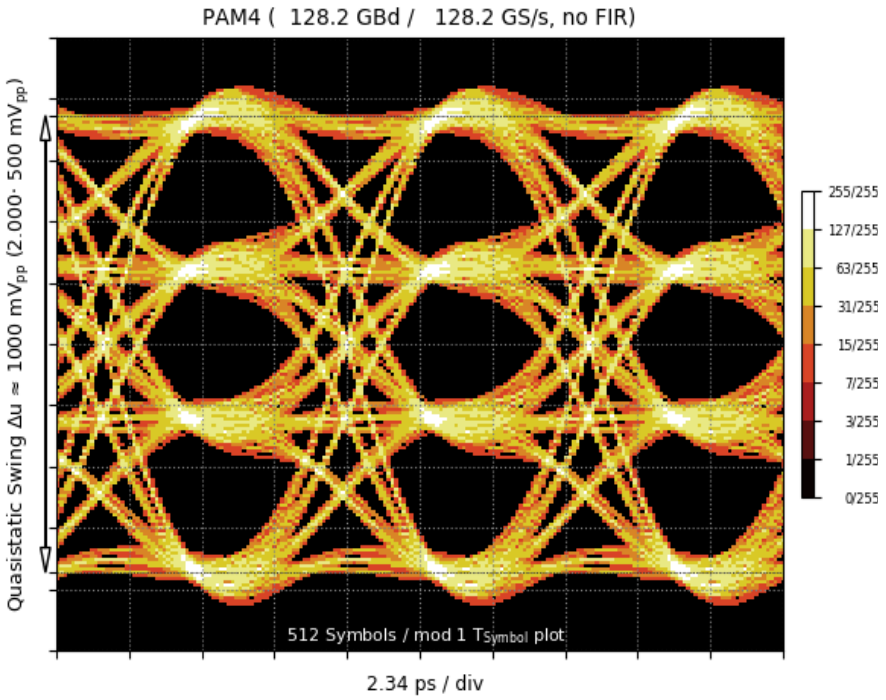


DAC Toplevel Layout
Die size ~ 5140 x 6042 µm²

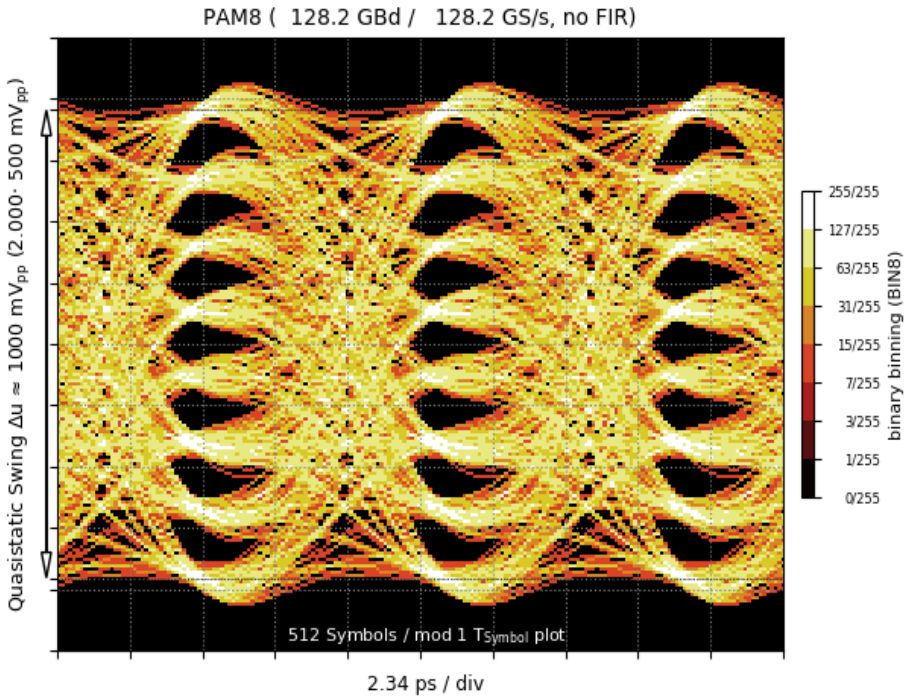


3.2 Single Core DAC: Simulated Eye Diagrams

PAM-4 (256 Gb/s) eye diagram at 128 GS/s



PAM-8 (384 Gb/s) eye diagram at 128 GS/s

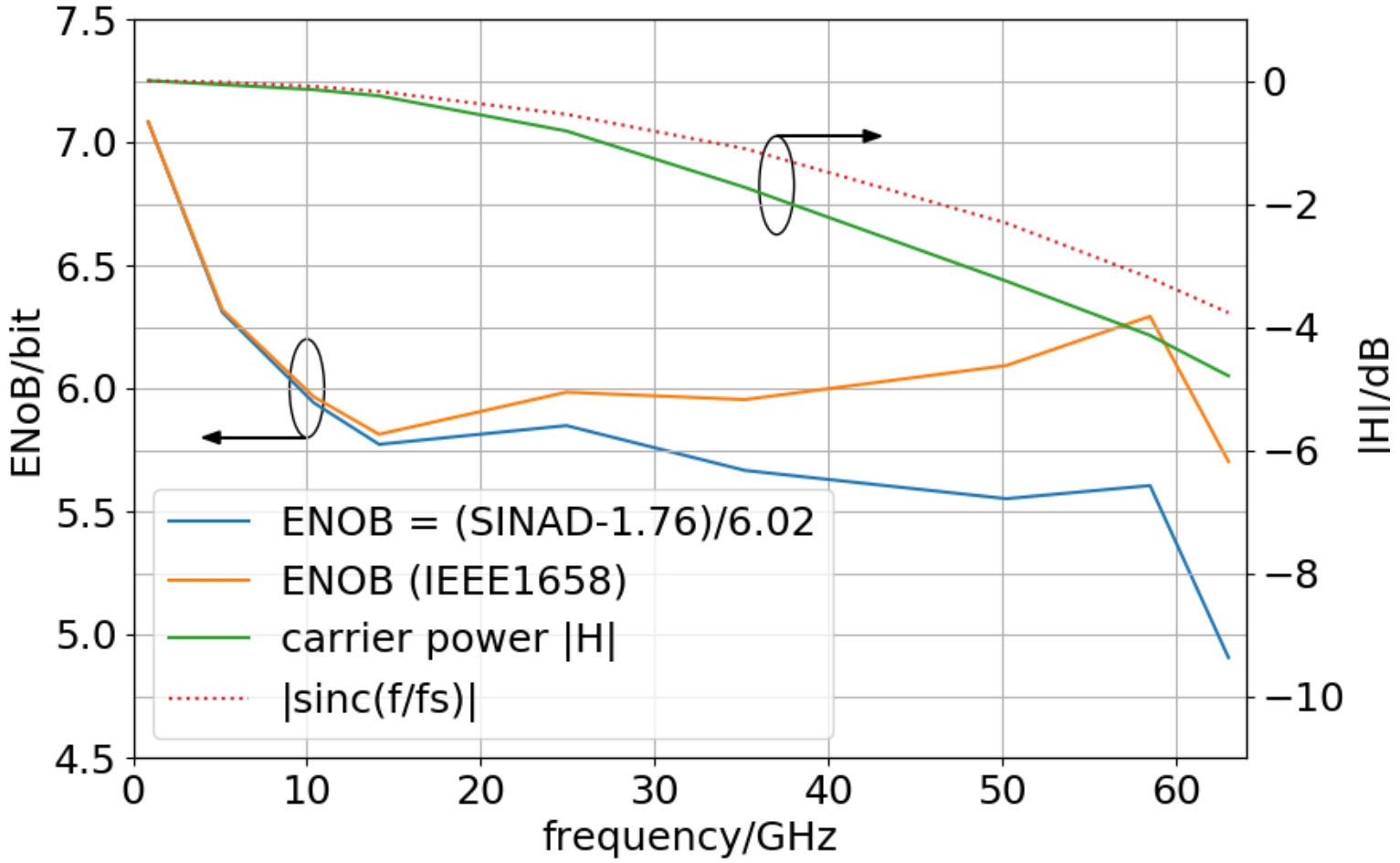


- Without assembly parasitics
- Pure DAC performance, no digital filter applied

3.2 Single Core DAC: Simulated Resolution & Bandwidth

Sinewave Synthesis results at 128 GS/s

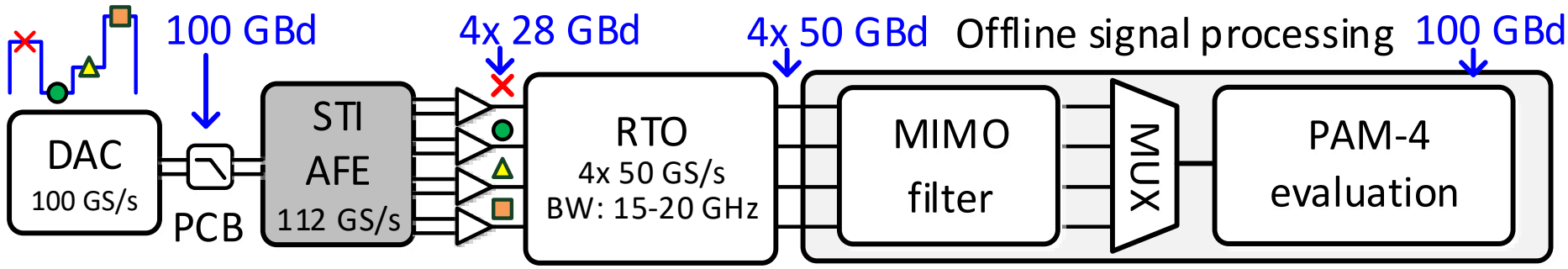
optimistic simulation without parasitics

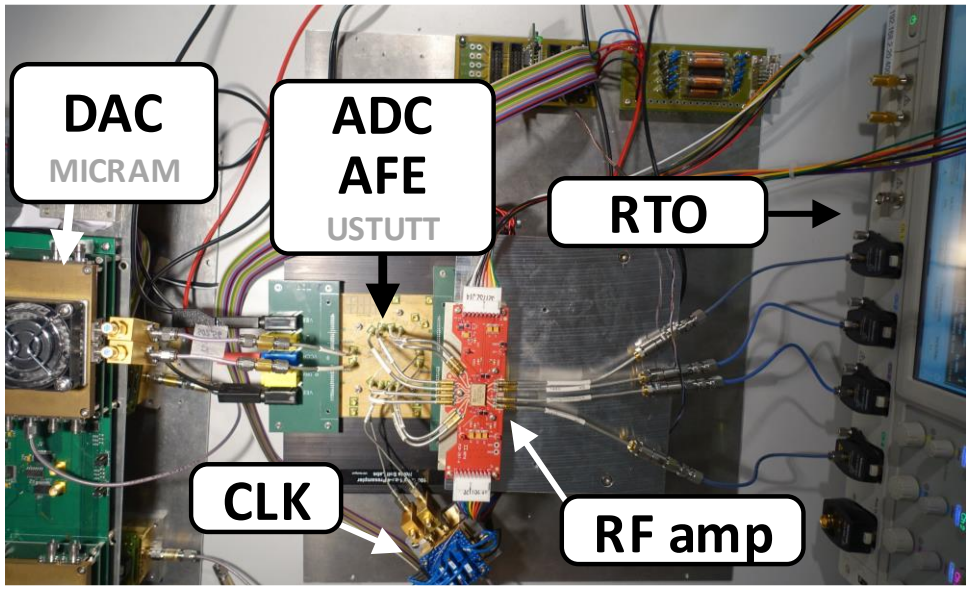


3.2 Single Core DAC: Summary

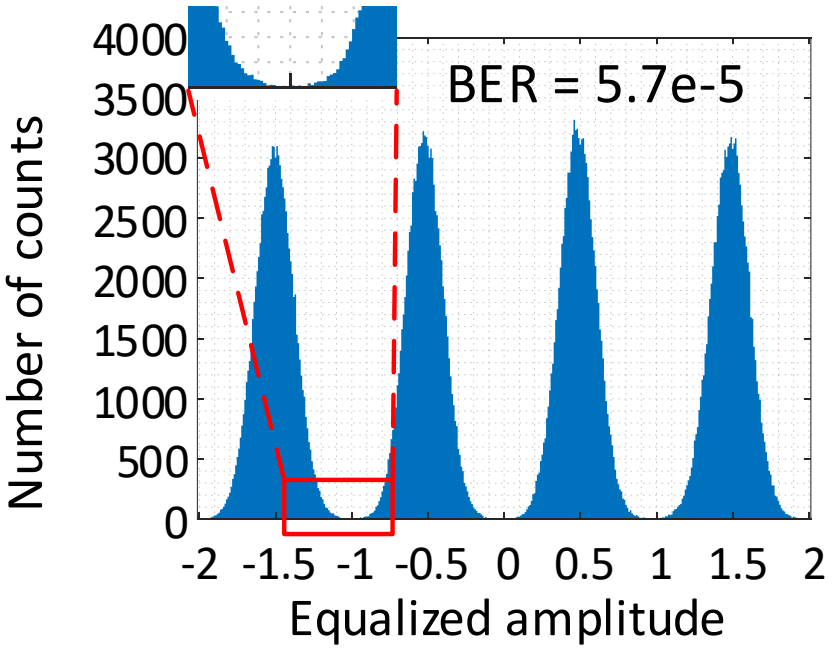
Parameter	Target Spec	optimistic simulation results/ implemented at Tapeout
Sampling Rate SR=1/T	**≥ 130 GS/s** as far as possible tunable	✓
Phys. Resolution	**8 bit**	✓
ENoB	**≥ 4** within 1st Nyquist band	**> 4.5** within 1st Nyquistband **> 5.5 up to 50 GHz** (without assembly parasitics)
Bandwidth	**> 50 GHz** (65 GHz targeted)	**> 70 GHz** (without substrate, flange connectors, …)
Full Scale Swing	**1 Vpp differential** (500 mVpp single-ended)	**400 mVpp … 1.2 Vpp differential**
Synchronization	**up to 4 DAC ICs**	Synchronization concept implemented
Pattern Memory Size	**≥ 512 kSamples**	**512 kSamples**

4. Application Experiments: Electrical B2B PAM4 (I)





PAM-4 test setup @ NOKIA-Lab

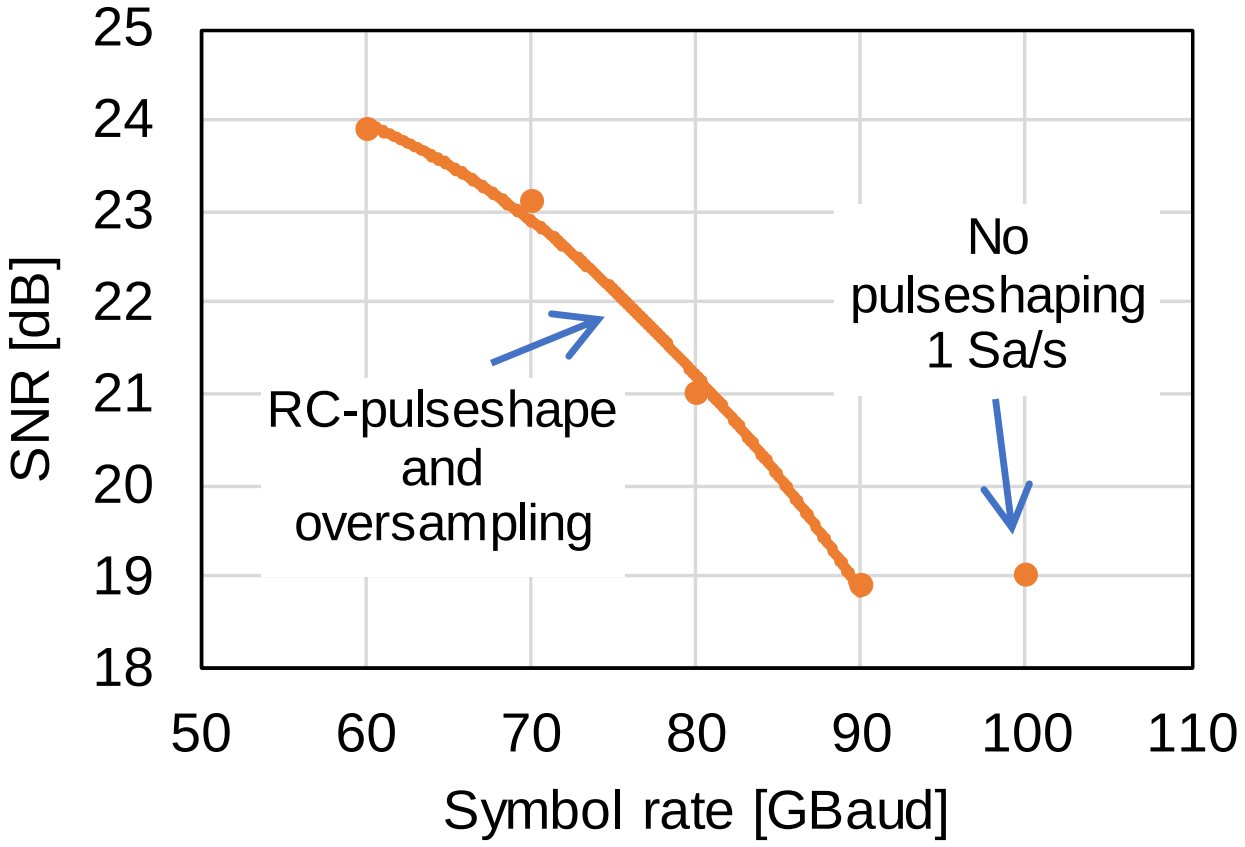


100 GBd PAM-4 (200 Gb/s)
Resampled symbols

X.-Q. Du, M. Grözing, A. Uhl, S. Park, F. Buchali, K. Schuh, and M. Berroth, "A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019),* Boston, MA, USA, 2019.

4. Application Experiments: Electrical B2B PAM4 (II)

- **Direct coupling of DAC to frontend**
- **PAM4 signal at variable symbol rate**
- **Oversampling in Tx for symbol rates <100 GBaud (different conditions in Tx)**
- **SNR 24 dB down to 19 dB of the end to end system**



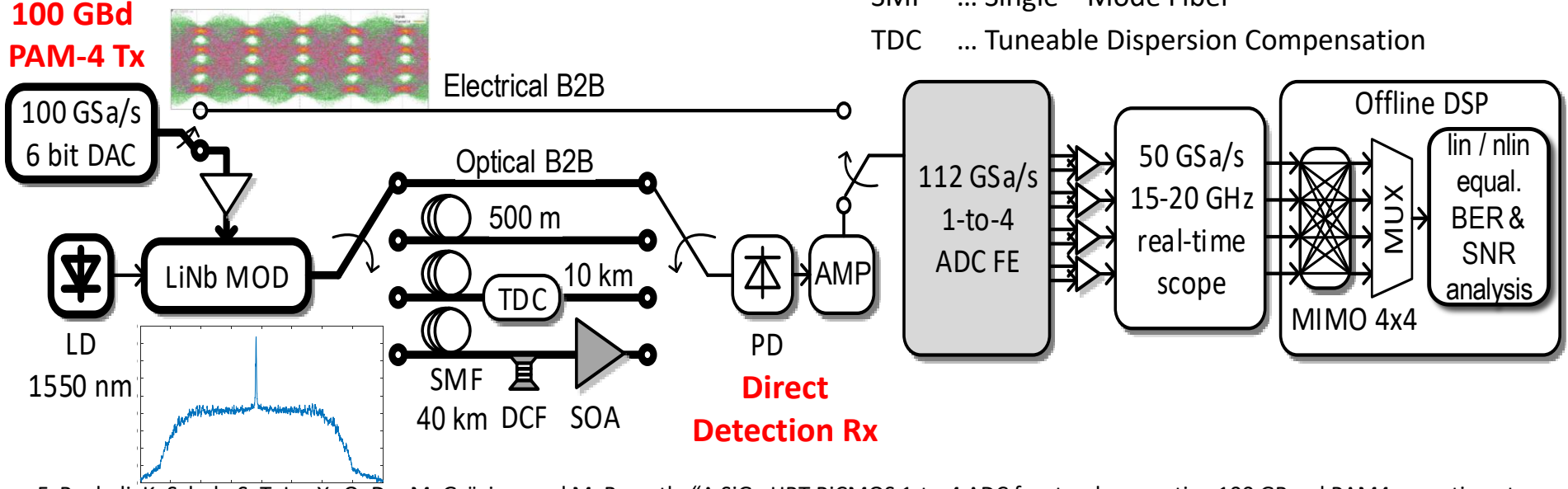
F. Buchali, K. Schuh, S. T. Le, X.-Q. Du, M. Grözing, and M. Berroth, "A SiGe HBT BiCMOS 1-to-4 ADC frontend supporting 100 GBaud PAM4 reception at 14 GHz digitizer bandwidth," in *2019 Optical Fiber Communication Conference (OFC 2019)*, 2019. https://doi.org/10.1364/OFC.2019.Th4A.7

4. Application Experiments: Optical PAM4 over Fibre (I)

- Tx
  - 100 GSa/s DAC + driver
  - LiNb amplitude modulator
  - Laser at 1550 nm, P_{out} up to 15 dBm
- Link
  - Data center reach = 500 m
  - Long reach = 10 km
  - Extended reach = 40 km
  - Chromatic fiber dispersion = 17 ps/nm/km

- Rx
  - High bandwidth PD, electrical amplifier
  - 1-to-4 ADC frontend, electrical amp with differential to single ended conversion
  - Sampling at 112 GSa/s, Nyquist frequency is >50 GHz
  - ADC at 50 GSa/s, bandwidth 14 GHz … 20 GHz

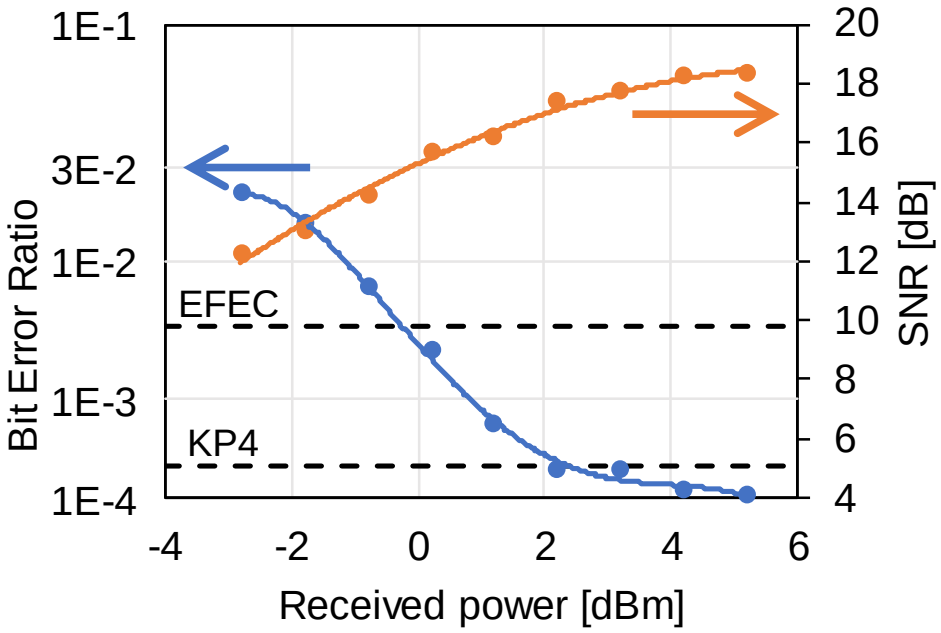
DCF … Dispersion Compensation Fiber
SOA … Semiconductor Optical Amplifier
SMF … Single -Mode Fiber
TDC … Tuneable Dispersion Compensation



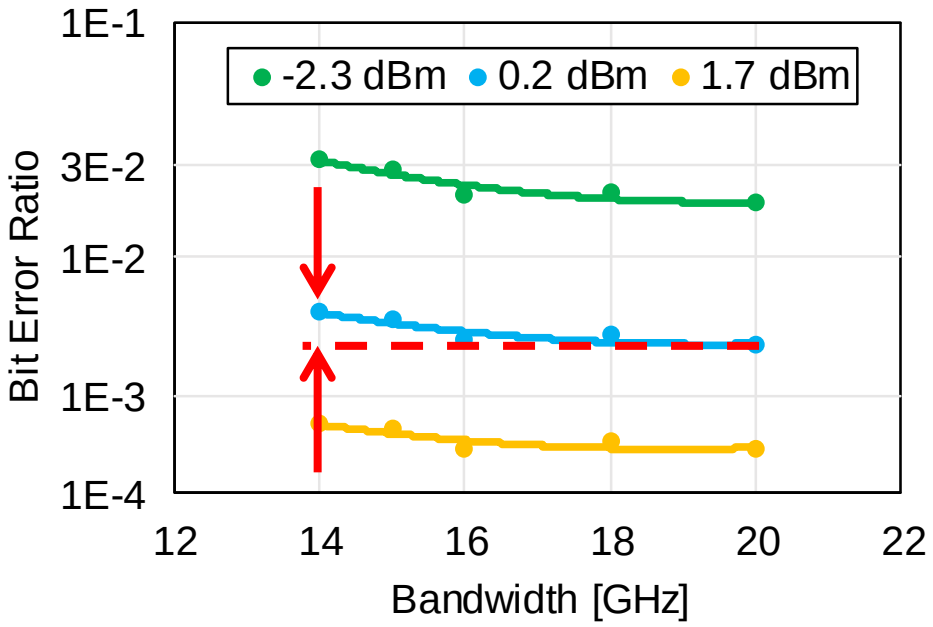
F. Buchali, K. Schuh, S. T. Le, X.-Q. Du, M. Grözing, and M. Berroth, "A SiGe HBT BiCMOS 1-to-4 ADC frontend supporting 100 GBaud PAM4 reception at 14 GHz digitizer bandwidth," in *2019 Optical Fiber Communication Conference (OFC 2019)*, 2019. https://doi.org/10.1364/OFC.2019.Th4A.7

4. Application Experiments: Optical PAM4 over Fibre (II)

Pre-FEC BER and SNR vs Rx power



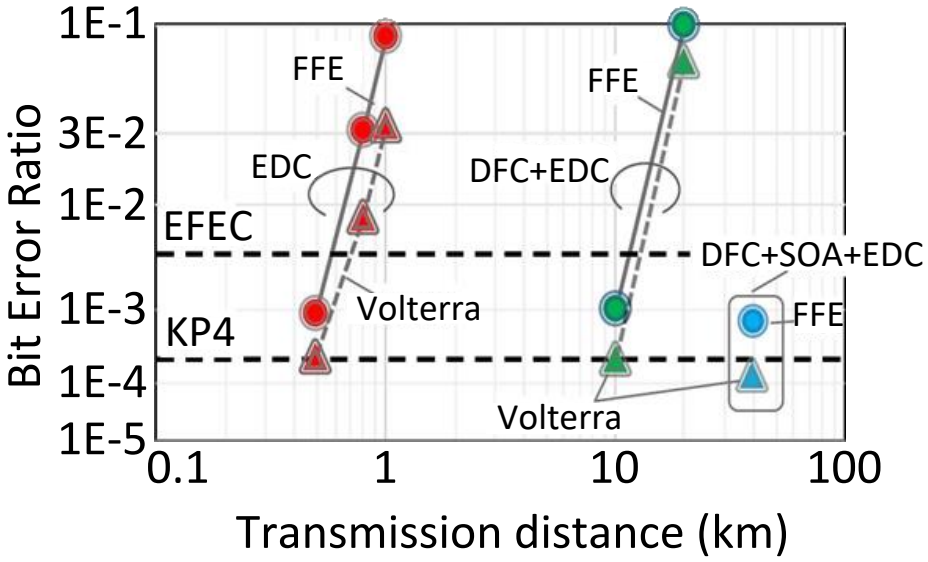
Pre-FEC BER vs ADC BW

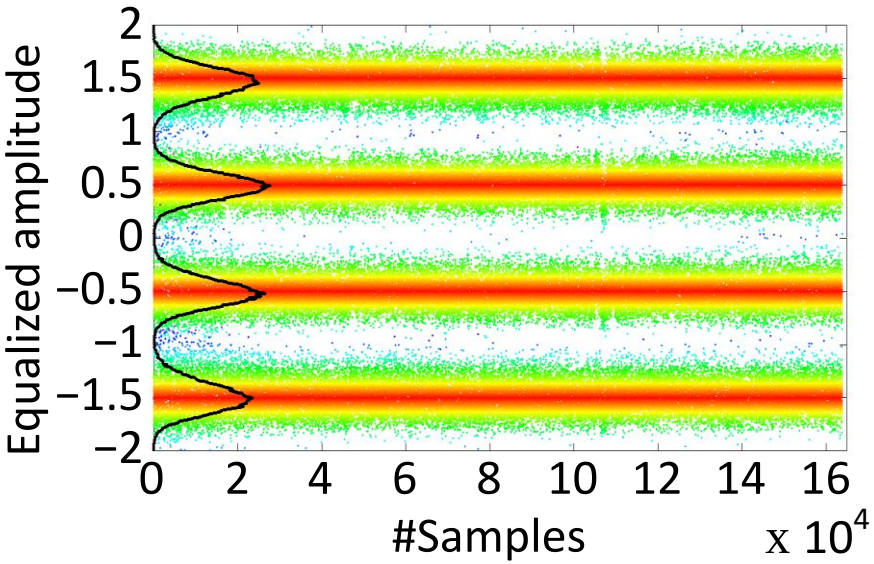


- **Requires +2.4 dBm and -0.3 dBm at KP4 and EFEC threshold**
- **SNR is slightly decreased by optical system by ~0.5 dB**
- **Down to 16 GHz bandwidth no power penalty, at 14 GHz 0.8 dB power penalty**

F. Buchali, K. Schuh, S. T. Le, X.-Q. Du, M. Grözing, and M. Berroth, "A SiGe HBT BiCMOS 1-to-4 ADC frontend supporting 100 GBaud PAM4 reception at 14 GHz digitizer bandwidth," in *2019 Optical Fiber Communication Conference (OFC 2019)*, 2019. https://doi.org/10.1364/OFC.2019.Th4A.7

4. Application Experiments: Optical PAM4 over Fibre (III)





BER below the EFEC threshold for

- 500m
- 10 km
- 40 km

Volterra

- mitigate residual nonlinearities
- improves BER below KP4
- gain is ½ decade in BER
- negligible gain in distance

100 GBd PAM-4 transmission with BER below the EFEC threshold with linear equalization and BER even below KP4 threshold with Volterra equalization

F. Buchali, K. Schuh, S. T. Le, X.-Q. Du, M. Grözing, and M. Berroth, "A SiGe HBT BiCMOS 1-to-4 ADC frontend supporting 100 GBaud PAM4 reception at 14 GHz digitizer bandwidth," in *2019 Optical Fiber Communication Conference (OFC 2019)*, 2019. https://doi.org/10.1364/OFC.2019.Th4A.7

5. Conclusion

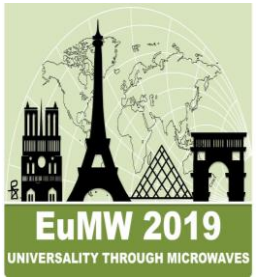
1. **Why SiGe-HBT Converter (-AFEs)?**

   Only SiGe-HBTs provide the necessary bandwidth

2. **A/D Conversion: Time-Interleaving Analog Front-Ends**
   1. STI 1:4 AFE (ADeMUX) @ 112 GS/s measured
   2. ATI 1:4 AFE concept for 40 GS/s designed & simulated
3. **D/A Conversion: Analog MUX and Single-Core Front Ends**
   1. STI 2:1 AFE (AMUX) for 128 GS/s designed & simulated
   2. Single-core DAC 128 GS/s designed & simulated
4. **A/D and D/A Application Experiment**

   100 GBd PAM4 (200 Gb/s) over 40 km with DD-Rx demonstrated below EFEC and KP4-BER-thresholds

Thank you



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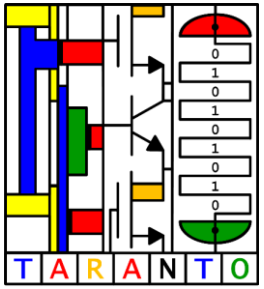

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