An Integrating Digitizer for an IR-UWB Receiver

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Abstract

A voltage integrator which is followed by a successive approximation register (SAR) analog-to-digital converter (ADC) for an impulse-radio (IR) ultra-wideband (UWB) receiver is presented in this paper. A sequence of wideband impulses carries information in IR-UWB systems which are used for short-range wireless communication and localization. The radio frequency (RF) frontend provides baseband impulses to the input of the proposed circuit. The first stage is an integrator that senses the impulses. Its output voltage depends on the number of received impulses and is converted to a digital code. The sequence of codes is passed to a digital processor that is able to retrieve the transmitted data.
The integrating analog-to-digital converter operates with a sampling frequency of 62.4 MS/s i.e. the integration period is about 16 ns. The core consumes 16.2 mA from a 2.6 V supply. The integrated circuit is fabricated in the 250 nm SiGe BiCMOS technology SGB25V from IHP.

1 Introduction

Presently UWB systems are the first choice for short-range medium data rate wireless transmission systems. They can coexist with other wireless systems because the transmitted power spectral density is low enough not to disturb narrow-band signals. In time-domain this wide-band signal consists of short impulses that have to fulfill the requirements given by the allowed frequency mask. The detection of the impulses can be realized very efficiently which makes low-power operation possible.
In [1] a SoC solution for IR-UWB receivers is presented. [2] realizes a complete receiver for 40 Mpulses/s. An SAR analog-to-digital converter for UWB achieving an SNDR of 25 dB at 125 MS/s is presented in [3].
The receiver with the integrating ADC operates according to the standard IEEE 802.15.4a. Not only data transmission but also localization is implemented in this system that is presented in [4]. The receiver is designed for a pulse rate of 500 Mpulses/s. Eight subsequent impulses are integrated and digitized by the proposed circuit which reduces the required ADC sampling frequency to 62.4 MS/s.
This paper is organized as follows: Section 2 describes the system setup and section 3 explains the realization of the circuit. Measurement results are given in section 4. Conclusions are drawn in section 5.

2 System Design

The proposed system consists of a voltage integrator that is followed by an analog-to-digital converter. An RF frontend similar to [5] receives a signal from an antenna and converts it to the baseband. This baseband signal contains a sequence of impulses that are applied to the integrator input. The output data of the analog-to-digital converter are passed to a digital processor.

2.1 Integrator

Eight impulses with amplitudes between -1 V and +1 V and a duration of 2 ns have to be integrated. Furthermore the integrator has to be reset after each integration period of 16 ns but must not have a dead time.
In order to provide integration without a dead time the integrator is designed as a twofold time-interleaved (TI) circuit as shown in Fig. 1. The input signal comes from the RF frontend and is distributed to two single integrators that are enabled alternately. At the end of the integration period the output signal remains constant and a multiplexer forwards it to the analog-to-digital converter.

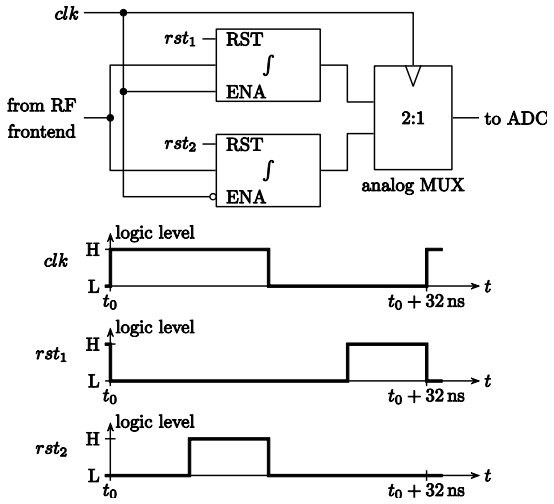

Fig. 1 Block and timing diagram of the TI integrator

The timing diagram is shown at the bottom of Fig. 1. The clock signal *clk* that controls the integrators and the multiplexer has a frequency of 31.2 MHz. Each integrator is reset before its integration phase by the signals rst_1 and rst_2. The reset phases have a length of 8 ns. The analog-to-digital converter has to sample the integrated signal after the integration is completed and before the reset phase begins.

2.2 Analog-to-Digital Converter

The ADC has a nominal resolution of 7 bit and a conversion rate of f_S = 62.4 MS/s. It is synchronized to the integrator so that it converts every output value of the integrator as soon as the integration is complete.

It consists of the SAR itself that stores the values of the bits D_6 (most significant bit, MSB) to D_0 (least significant bit, LSB). A switched-capacitor (SC) digital-to-analog converter (DAC) and subtractor determines the difference of the analog input voltage and its digital representation in the SAR. The polarity of this difference is detected by a comparator whose output controls the SAR. This enables the successive determination of the digital code by means of a binary search.

3 Circuit Design

The circuit is realized in the 250 nm SiGe BiCMOS process SGB25V from IHP. Fig. 2 shows a photograph of the die that has a size of 1.4 x 0.6 mm^2. The integrator occupies an area of 90 x 210 µm^2 and the analog-to-digital converter 360 x 280 µm^2.

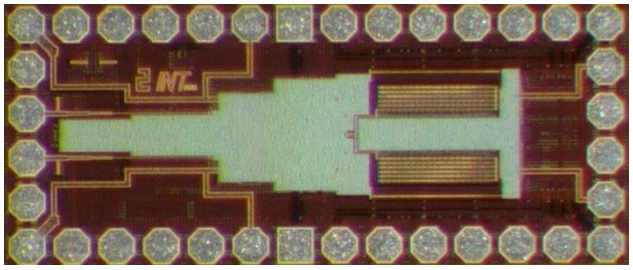

Fig. 2 Chip photograph

Besides the integrator, multiplexer and analog-to-digital converter the chip contains a clock input amplifier, a clock divider and output drivers.

3.1 Integrator

Each integrator is realized with an operational amplifier (op-amp) with capacitive feedback and input resistors R_{in}. The time constant is dimensioned for the voltage input range of the following analog-to-digital converter to be fully covered. The inputs can be isolated by serial MOS switches controlled by an enable signal *ENA*. To reset the integrator the metal-insulator-metal integration capacitors are short-circuited by MOS switches controlled by *RST*.

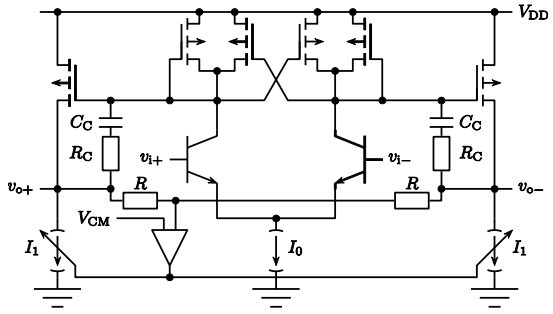

Fig. 3 Operational amplifier

A simplified circuit diagram of the two-stage op-amp is shown in Fig. 3. The first stage is a differential amplifier with a bipolar differential pair providing better matching properties, a larger transconductance and a larger transit frequency than MOSFETs. A comparison to a former op-amp shows that the rms value of the amplifier's offset voltage is five times smaller if the input is realized with bipolar transistors instead of MOSFETs.
The second stage consists of two single-ended common-source circuits. Stability is ensured by a RC Miller compensation from the output of the second stage to its input. Common-mode control is realized by an additional amplifier that adjusts the current sources in the second stage.
The multiplexer connecting the outputs of both integrators to the input of the single ADC is realized by a pair of p-channel transfer transistors. Two multiplexers are needed because of the differential circuit design.

3.2 Analog-to-Digital Converter

The sampling period is one clock cycle of the 499.2 MHz clock and the binary search algorithm takes seven clock cycles. Due to the large input capacitance of the SC-DAC and the short sampling period emitter followers are applied to the interface between the MUX and the ADC.
The SAR consists of fully differential flip-flops in CMOS technology. They control the timing of the switching algorithm and store the values of each bit at the same time.
All unit capacitors in the SC-DAC are designed with a basic building block. Each block has a metal-insulator-metal (MIM) capacitor and several transfer gates that enable to switch between the input voltage, a positive or a negative reference voltage. Using equal building blocks is important for matching and uniform parasitic capacitance.
The comparator has two stages. The first stage is a differential amplifier that reduces kickback from the comparator output to the SC-DAC and preamplifies the DAC output signal. The second stage is similar to [6] with a cross coupled n-channel MOSFET pair.
All reference voltages are generated on-chip with an op-amp as shown in Fig. 3, the outputs buffered with emitter followers. The desired output common-mode voltage is applied to the op-amp's control input by an on-chip resistive voltage divider but can be changed from outside. The input range is given by the difference of both reference voltages which is controlled by the voltage input V_{BGP}. This voltage is generated with an on-chip resistive voltage divider as well but the input is designed to be connected to a bandgap reference.

4 Measurement

The whole chip consumes 130 mA from a 2.6 V supply. The output drivers consume 70 mA, the core (integrator and analog-to-digital converter) 16.15 mA. The integrator consumes 2.15 mA, the analog-to-digital converter 5 mA and the emitter followers 9 mA including a reference current source. The op-amp that generates the reference voltages consumes 900 µA. The rest is consumed by resistive voltage dividers for 50 Ω input matching.

4.1 Integrator

The differential output voltage V_{oD} of the integrator is measured for constant differential input voltages V_{iD} of variable values. The difference of the measured value and the ideal value is divided by the full range and yields the integrator's nonlinearity that is shown in Fig. 4. The

"noise" of the measurement curve is caused by the digital oscilloscope that is used to measure the integrator output which is periodically reset.

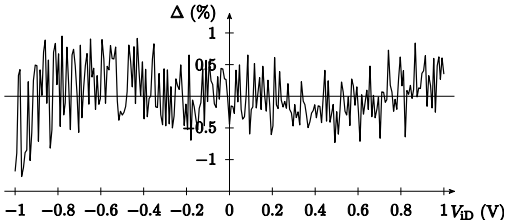

Fig. 4 Integrator measurement: nonlinearity

The nonlinearity is smaller than 1.5 % all over the integrator range. The receiver in [4] only utilizes positive voltages where the nonlinearity is smaller than 1 %. This error corresponds to a resolution of 6 bit and hence satisfies the requirements.

To verify the integrator's ability to indicate the number of received impulses a bit sequence is applied to the input that includes all 256 combinations of eight impulses being "H" or "L" during one integration period. Fig. 5 shows the output voltage versus the number of (in this case negative) "H"-impulses. The measurement shows that the output voltage clearly indicates the number of impulses which makes the integrator applicable for the receiver.

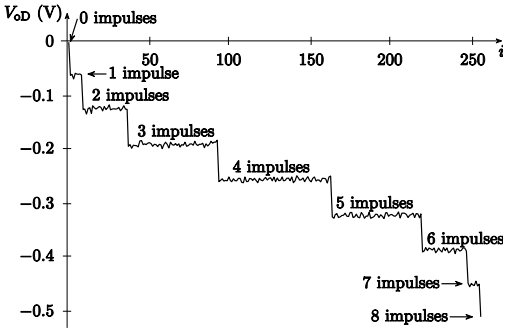

Fig. 5 Integrator measurement: Various pulse sequences (62.4 Msymb/s)

4.2 Analog-to-Digital Converter

The effective number of bits (*ENOB*) measurement for the 7 bit 62.4 MS/s SAR ADC is shown in Fig. 6. According to [4] an effective resolution of 4 bit is sufficient for the application. As only half of the converter's range is used in a non-coherent receiver *ENOB* > 5 must hold at least up to Nyquist frequency f_{Ny} = 31.2 MHz. Fig. 6 shows that this requirement is fulfilled because the effective resolution is larger than 5.7 bit up to 100 MHz.

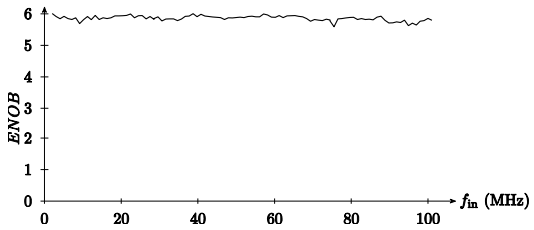

Fig. 6 ADC measurement: *ENOB* (62.4 MSymb/s)

For the serial connection of the integrator and the ADC the capability to indicate the number of received impulses is investigated similarly to the dynamic measurement in Section 4.1. The digital output data is recorded by a logic analyzer. The results are shown in Fig. 7.

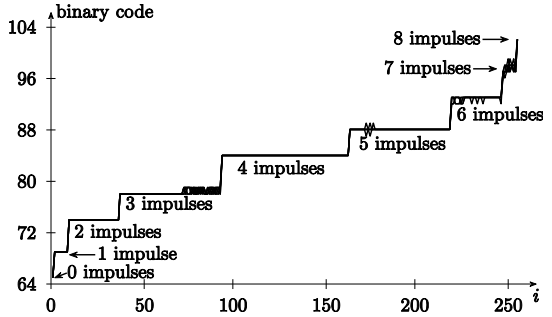

Fig. 7 Integrator and ADC measurement: Various pulse sequences (62.4 MSymb/s)

Certain numbers of impulses cause distinctive output codes which enables to detect the numbers of impulses. A variation of ±1 LSB occurs for some impulse numbers which happens if the integrated voltage is near a quantization threshold of the analog-to-digital converter.

5 Conclusion

An integrating digitizer for an IR-UWB receiver according to the standard IEEE 802.15.4a is proposed. The received and down converted signal is integrated and then digitized which enables the reconstruction of the transmitted data. Measurement results show that the requirements given in [4] are fulfilled. The integrator has a linear transfer characteristic and the effective resolution of the analog-to-digital converter exceeds 5 bit up to Nyquist frequency. Thus the number of received impulses can be recovered.

The integrator reduces the pulse rate of 499.2 Mpulses/s to a symbol rate of 62.4 Msymb/s. The SAR ADC has a conversion rate of 62.4 MS/s and digitizes the received signal. The core components integrator, analog MUX and SAR ADC consume 16.15 mA from a 2.6 V supply.

6 References

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