SiGe Bipolar Limiting Amplifier with a Bit Rate of 50 Gbit/s for Optoelectronic Receivers

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Fast Ge on Si p-i-n photodiodes (PDs) suitable for a bit rate of 25 GBit/s have been presented [1]. In order to reduce the required optical input power, a differential limiting amplifier (LA) has been designed which will be placed between the PD and the flip flop (FF) used in [1]. The design of the LA is realized in a bipolar SiGe technology (B7HF200) from Infineon with a transit frequency f_T of 200 GHz.

At an optical input power of 1 mW, the output voltage of the PD is 1 mV at a 50 Ω load. To drive the FF, the LA has to provide a voltage gain of 300. The PDs have a 3 dB bandwidth of 49 GHz [2]. The minimum targeted bit rate for the LA is hence 50 Gbit/s.

Fig. 1 shows the circuit topology and layout of one amplifier stage. One driver (DRV) stage consists of a differential amplifier (DA) and an inductor for inductive peaking (INP) [3]. An emitter follower (EF) in front of the DRV prevents the DA from saturation. Six DRV stages with preceding EFs are used in total, each with a gain of 3. The first 4 stages work at 4 mA, the 5th at 6 mA and the 6th at 12 mA to drive 50 Ω-loads differentially with a voltage swing of ±300 mV.

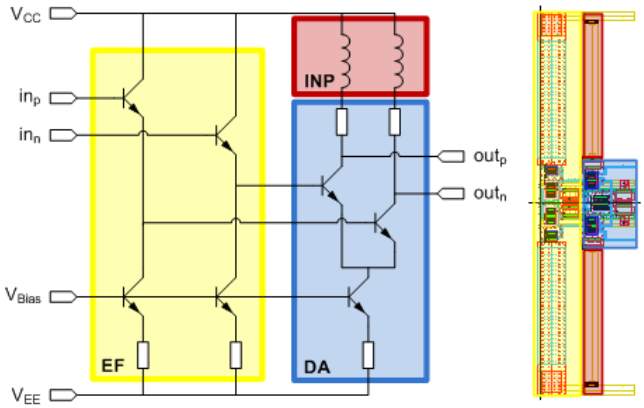

Fig. 1: Circuit topology and layout of one 4 mA-stage.

The whole chip in Fig. 2 has a size of 580 x 580 µm². Four times four pads with a pitch of 100 µm are used for RF-probe contacting.

The measurement setup is similar to the one described in [1]. The generated electrical high-speed pseudo random bit sequence (PRBS) is attenuated and then fed to the LA input.

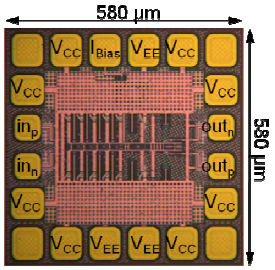

Fig. 2: Photograph of the overall chip.

Measurements with single-ended and differential input are done. One output of the LA is connected to a sampling oscilloscope to monitor the eye diagram as shown in Fig. 3. The circuit draws 100 mA at a supply voltage of -3.1 V. The input voltage swing of the LA is 45 mV and ±45 mV for single-ended and differential signals, respectively, which results in a differential output voltage swing of ±300 mV. A lower input voltage cannot be provided by the measurement setup due to bandwidth-limited attenuators.

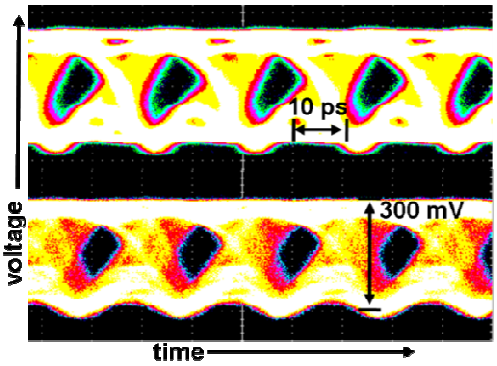

Fig. 3: Eye diagram of the LA output signal with single-ended (top) and differential (bottom) input at a bit rate of 50 Gbit/s.

50 Gbit/s are achieved for both, single-ended and differential input, with a PRBS length of 2^{31}-1. As a next step, the LA will be measured together with the PD.

[1] S. Klinger et al., *ECOC 2009*, Paper 9.2.3, Vienna/Austria, 20-24 September 2009.
[2] S. Klinger et al., *IEEE-PTL*, vol. 21, no. 13, pp. 920-922, July 2009.
[3] B. Razavi, "Design of Integrated Circuits for Optical Communications", McGraw-Hill New York, 2003.