

12.5 Gbit/s Configurable Threefold 2:1 MUX and 1:2 DEMUX Chips in 130 nm CMOS Technology

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Abstract— A threefold 2:1 multiplexer (MUX) Chip and a 1:2 threefold demultiplexer (DEMUX) Chip for data rates up to 12.5 Gbit/s are presented. The chips are designed for interfacing 6 bit 25 GS/s DACs/ADCs with an FPGA. The input sampling time and the outputs delay can be adjusted to synchronize the data using programmable registers on chip. The MUX and DEMUX chips are implemented in 130 nm CMOS technology.

I. INTRODUCTION

The MUX and DEMUX chips are designed for testing 25 GS/s 6-bit digital-to-analog converters (DAC) [1] and analog-to-digital converters (ADC) [2] with input and output data interfaces with 12.5 Gbit/s/channel. A field-programmable gate arrays (FPGA) with multi-gigabit transceivers (MGTs) is employed to transmit and receive the digital signal. For example, the Xilinx Virtex4 series offers a data rate up to 6.5 Gbit/s at up to 24 differential channels. With the MUX and DEMUX Chips two channels can be combined to a single 12.5 Gbit/s channel to half the number of the required interfaces on the DAC and ADC chips. However, data synchronization between two FPGA MGT channels is a difficult task. Therefore, the input sampling time and the output delay of both chips are designed to be configurable using programmable registers. These registers enable an automatic synchronization controlled by the FPGA. The MUX and DEMUX chips are also suitable for testing other digital interfaces. Both chips are designed in 130 nm CMOS technology.

II. CHIP DESIGN

To achieve a high clock frequency, current mode logic (CML) is employed. The power consumption of the MUX chip and the DEMUX chip are 1.6 W and 1.4 W with a supply voltage of 1.5 V.

A. MUX Concept

The 2:1 MUX block consists of 5 latches and a 2:1 MUX [3]. The latches delay the two inputs with 180° phase shift, since the input signals should be stable during the time, at which it connects to the output. Fig.1 shows the block diagram of the MUX chip. There are three MUX blocks integrated on one MUX chip. The positive output voltage level (1.5 V ~ 1 V) of FPGA MGTs is shifted down to the negative input voltage level (0 V ~ 400 mV) of the DAC, using a level-shifter. Therefore the MUX chip has 3 supply voltages, 1.5 V, 0V and -1.5 V. The input-synchronizer is able to sample the digital inputs individually or globally at the four different phases 0°, 90°, 180° and 270°. The MUX block with 2 input-synchronizers is shown in Fig.3. The outputs can be operated at two phase (0°, 180°). The XORs are used to verify the synchronization of the inputs of the MUX blocks. Fig.4 shows the block diagram of the XORs. FPGA transmit the same PRBS on all channel of MUX chip. Each two adjacent channels are connected to one XOR, and the XOR outputs can be selected to be connected to the pulse stretcher. The pulse-

stretcher detects unsynchronized data and generates a long pulse at the output [2]. The XORs, the input-synchronizers and the phase-selector are controlled by a programmable register. The 1:2 frequency divider generates an internal clock signal with phases. A reference clock for the FPGA MGTs is generated by 1:16 frequency divider.

B. DEMUX Concept

The DEMUX consists of 5 latches. The input data are sampled with either rising edge or falling edge of the clock, and held for one clock period. The first sampled data are delayed for a half clock cycle to be synchronized with the second one. The block diagram of the DEMUX chip is shown in Fig.2. Similar like the MUX chip, three DEMUX blocks are integrated on one DEMUX chip. The negative voltage level of ADC is shifted up to match the input voltage level of the FPGA MGTs. The input sampling time can be set to two phase (0°, 180°). The DEMUX outputs can be set individually or globally to the four different phases (0°, 90°, 180° and 270°), so that the FPGA can adjust the sampling time of each individual DEMUX output channel. The phase selection is also controlled by the programmable register.

III. LAYOUT

The layout of the MUX and DEMUX chips are shown in Fig.5 and Fig.6. The chip area of each chip is 0.4 x 2.3 mm².

IV. MEASUREMENT RESULTS AND CONCLUSION

The first measurement of these chips is done on-wafer. Fig.7 shows the measured eye-diagram of one MUX output with a data rate of 12.5 Gbit/s. The input clock is 12.5 GHz, and the input pattern are two 6.25 Gbit/s 2³¹-1 pseudo random bit sequences (PRBS). The eye opening is 70 ps horizontally and 250 mV vertically. Fig.8 shows the measured eye-diagram of two DEMUX outputs with a data rate of 6.25 Gbit/s each. The input clock is 12.5 GHz, and the input pattern is a 12.5 Gbit/s 2³¹-1 PRBS. The eye opening is 150 ps horizontally and 300 mV vertically.

The MUX and DEMUX chips are presented. They enable the connection of converters with 12.5 Gbit/s interfaces with 6.25 Gbit/s MGT on FPGAs. A redesign in 90 nm CMOS will enable the connection of 32 GS/s converters with 16 Gbit/s interfaces with 8 Gbit/s MGT on FPGAs.

REFERENCES

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- [2] Felix Lang, T. Alpert, M. Grözing, M. Berroth, "Design of a 25 GS/s 6-bit Flash-ADC in 90 nm CMOS technology" ESSCIRC 2009 Fringe (European Solid-State Circuits Conference Fringe), Athens, Greece, September 14-18, 2009.
- [3] Razavi, Behzad: Design of integrated Circuits for optical communications. McGraw-Hill, 2003

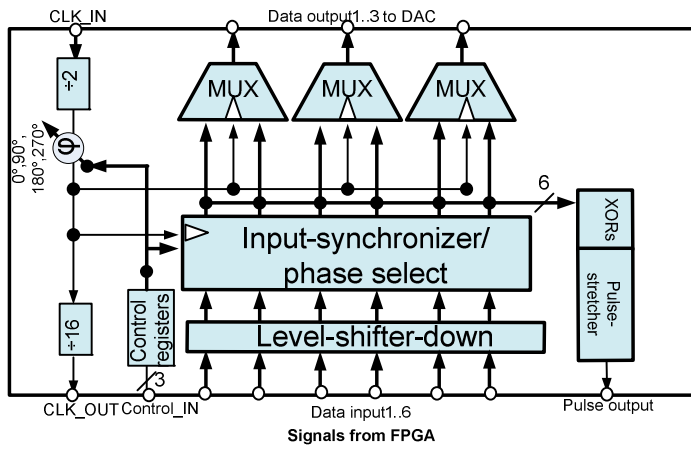


Figure 1. block diagram of MUX Chip

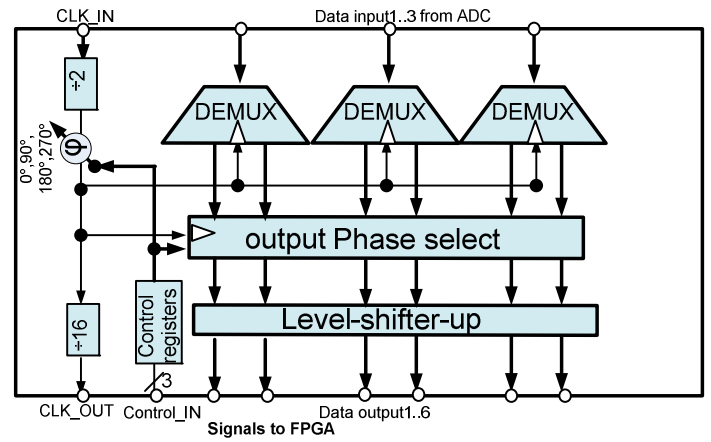


Figure 2. block diagram of DEMUX Chip

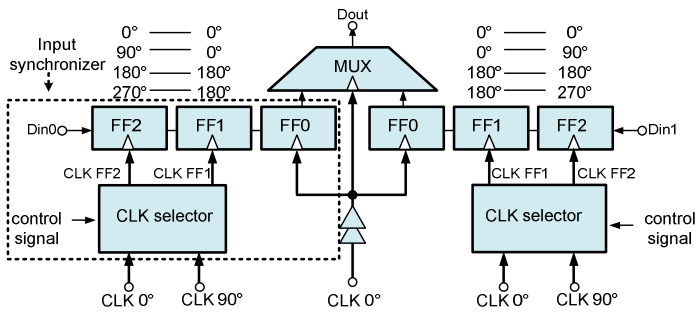


Figure 3. Block diagram of MUX with input synchronizer

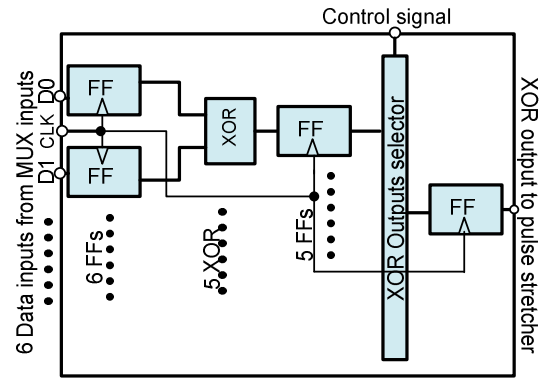


Figure 4. Block diagram of the XORs block

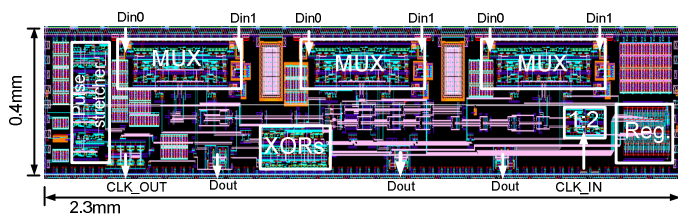


Figure 5. Layout of MUX Chip

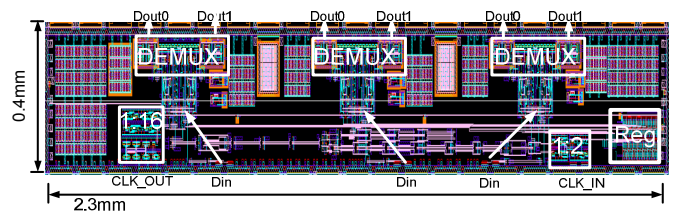


Figure 6. Layout of DEMUX Chip

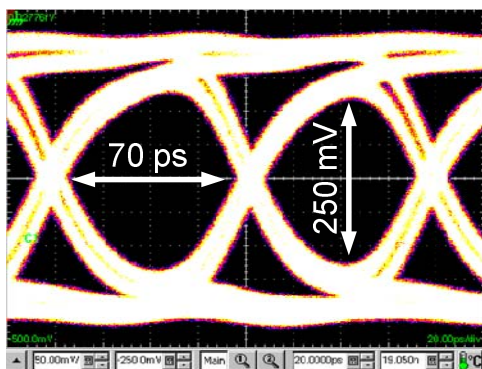


Figure 7. Eye diagram of a MUX output at 12.5 Gbit/s for two inputs with 6.25 Gbit/s $2^{31}-1$ PRBS.

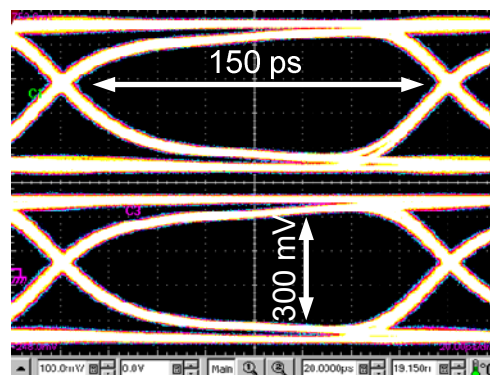


Figure 8. Eye diagram of two outputs of a DEMUX at 6.25 Gbit/s for an input with 12.5 Gbit/s $2^{31}-1$ PRBS.