

Fig. 2. Capacitor bank with for tuning and modulation.

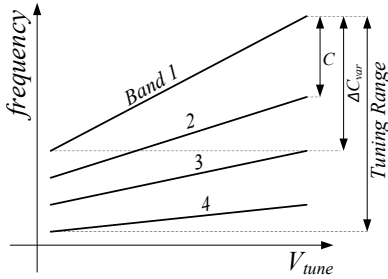


Fig. 3. Tuning characteristic of a 2 bit capacitor bank.

together the source and drain of a MOS transistor making it a two terminal device ( $M_{n\{1,2\}}$  in fig. 2). The capacitance of this component consists of the oxide capacitance, which is fixed, plus the depletion capacitance which is proportional to the voltage drop across the device terminals [3].

### B. Discrete Frequency Tune

The use of pass-gate logic allows the switching-on or off of capacitors thereby resulting in discrete changes of frequency. It can be seen in fig. 2 that two such *switched* capacitors are used and it results in a 4-band tuning characteristic. In order to have a uniform change of frequency between each of the frequency bands, the capacitors are binary weighted such that when the digital tune values  $V_{dig0}$  and  $V_{dig1}$  are 00 the bank capacitance is equal to 0, when it is 01 the capacitance is equal to  $C$ ,  $10 \rightarrow 2C$ , and  $11 \rightarrow 3C$ . Additionally, the frequency is continuously tuned within each frequency band by the utilization of varactors. Use of the described discrete frequency variation has the following advantages [2]:

- 1) Increases tuning range.
- 2) Avoids frequency instability and sensitivity to input noise since it lowers the tuning sensitivity ( $K_{VCO}$ ).
- 3) Lowers power consumption.
- 4) Improves phase noise.

The MOS switches are designed with reduced power dissipation in mind. For that reason, only one pass-transistor is used

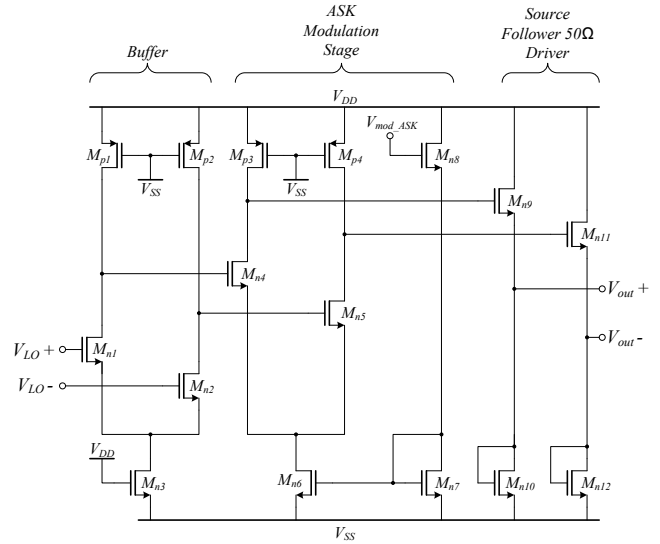


Fig. 4. Differential ASK modulation and output stage used in the cross-coupled oscillators and the differential ring oscillators.

for switching, and the structure is made symmetric by using two capacitors, which have lesser parasitic losses, as shown in fig. 2. Placement between the capacitors moves the transistor parasitics away from the oscillation nodes thus improving the resonator quality factor (Q). Note the transistors connected to VSS at the switch transistor's source and drain, these are placed in order to ensure the voltages at those terminals are according to correct operation since they are otherwise floating nodes.

The plot in fig. 3 clarify the 4 frequency bands resulting from the capacitor bank, it can be observed that  $K_{VCO}$  decreases when more capacitors are appended since the variable varactor capacitance ( $\Delta C_{var}$ ) becomes a smaller fraction of the total capacitance. As shown on the figure, the overlap between the frequency bands is controlled by varying  $C$  while the tuning range within each band is controlled by the varactor's  $\Delta C_{var}$  [2].

### C. Frequency Shift Keying (FSK) Modulation

FSK modulation is a variant of digital modulation in which the digital "0" and "1" are each assigned a frequency at a small offset from one another. This can be done by controlling the voltage on the analog tune control, however this has the drawback of high error-rate due to noise sensitivity and small frequency offset required for modulation. This problem is circumvented, as it can be seen from fig. 2, by using a small varactor dedicated for digital modulation input [3], [4]. Placing two small varactors back-to-back means that the variable capacitance is halved due to the series combination, which lowers the frequency offset to the required value of  $\pm 100$ -kHz.

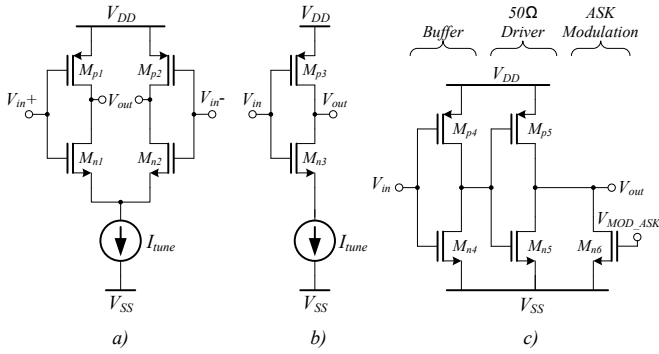


Fig. 5. A CMOS a) differential and b) single-ended inverter. c) CMOS output stage used in the single-ended ring oscillator.

#### D. Buffer, Amplitude Shift Keying (ASK) Modulation Stage and Output Driver

The output stage is designed to drive a 50-Ω load, which is also the termination of most measurement equipment. A buffer with small input transistors is placed to isolate the local oscillator (LO) signal and avoid frequency pulling. Optional ASK modulation is possible by varying the current through a current mode logic (CML) amplifier as shown in fig. 4. This is followed by a source follower with large transistors to provide enough current for the 50-Ω load.

### III. RING VCO DESIGN

CMOS configuration is preferred to other common-source or CML topologies since it has lower power consumption and maintains the amplitude of oscillation very well across a wide range of frequencies when tuned through the tail current ( $I_{SS}$  in fig. 5). Using this method of tune, the frequency is tuned virtually from DC up to the maximum ring frequency [5].

For the differential ring oscillator the same output stage in fig. 4 is used. As for the single-ended one, a CMOS output stage is designed with the same basic components. A small CMOS inverter is used to buffer the oscillator from the driver and load. This is followed by another inverter with larger transistors to provide enough current for the 50-Ω termination. ASK modulation is done simply by connecting a pull-to-ground transistor at the output. It is sized with respect to the driver inverter in order to control the output amplitude with modulation ratio 1:3.

### IV. SIMULATION RESULTS

#### A. Cross-Coupled VCOs

The plot in fig. 6 shows the frequency tuning characteristic for the 2.45-GHz cross-coupled VCO. The four tuning curves are a result of the possible switching of the 2-bit capacitor bank array, and since there are two branches, there are  $2^2 = 4$  possible tune values. A frequency tune ratio of about 35% is achieved, from 2.05-GHz up to 2.90-GHz. The  $K_{VCO}$  for each tuning band increases when moving from a lower band to a higher one with an overall  $K_{VCO}$  of 125-MHz/V. Although across the whole voltage range the tuning linearity is poor, it

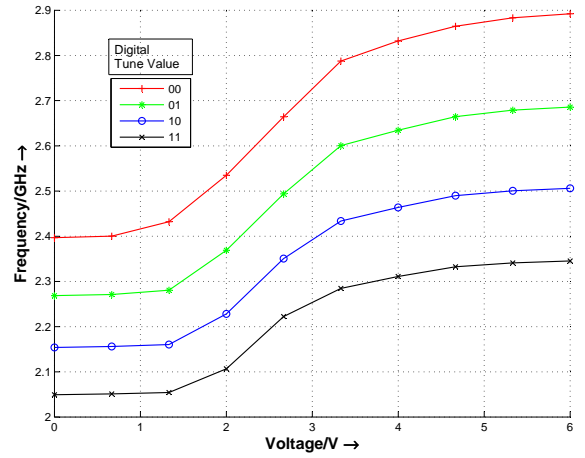


Fig. 6. Frequency tuning curves for the 2.45-GHz cross-coupled VCO.

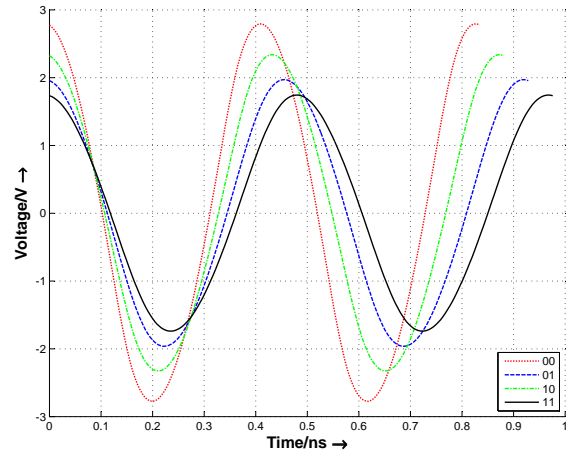


Fig. 7. LO waveform across different digital tune values for the 2.45-GHz cross-coupled VCO.

improves greatly if a smaller range (1.3V – 3.4V) is chosen. Similar results are obtained for the 900-MHz VCO.

Fig. 7 shows the variation of the LO waveform amplitude across the four frequency bands. It is observed that the amplitude decreases with frequency, this change in amplitude can be explained by the extra losses introduced by turning on more of the non-ideal MOS switches.

Power consumption of the 2.45-GHz VCO is 23-mW with a tail current of 5-mA. The output stage consumes 34-mW of power and the transmitter is able to deliver about 100-mW to a 50-Ω load. For the 900-MHz VCO, larger transistors were used in realizing a bigger negative transconductance component. This is to compensate for the greater losses found at the lower frequency used, since the passive components have lower Qs at lower frequencies. For this reason the power consumption for the 900-MHz VCO core is higher: 60-mW at 15-mA tail current.

The spectral purity of the cross-coupled VCO is very good when compared to the ring VCOs. The first harmonic component is only about -30-dBm as shown in fig. 8, while that value is greater than zero for both ring VCOs. Phase noise

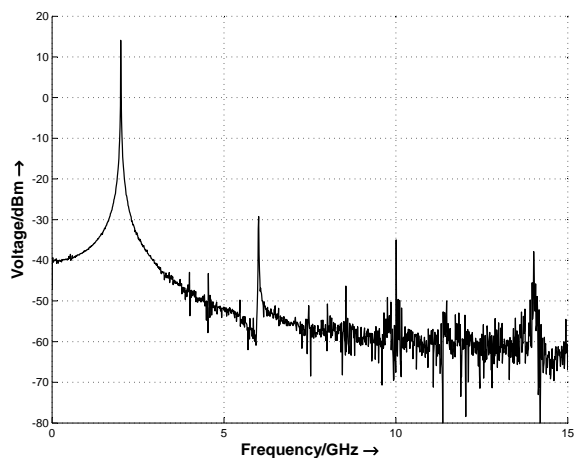


Fig. 8. LO harmonic spectrum of the 2.45-GHz cross-coupled VCO.

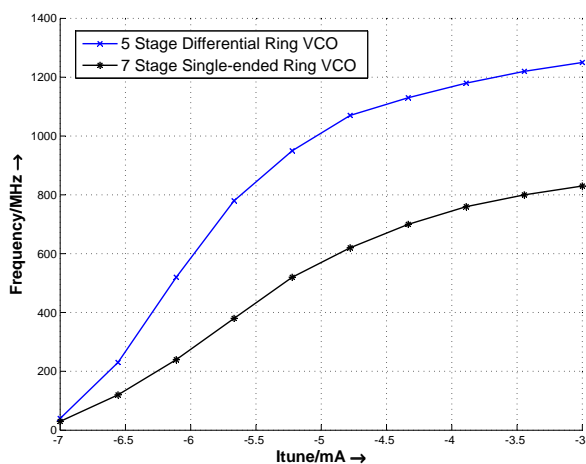


Fig. 9. Frequency tuning curves for the ring VCOs.

is simulated at  $-65$ -dBc/Hz at 100-kHz offset frequency.

### B. Ring VCOs

The tuning characteristic of the ring VCOs are shown in fig. 9. Ring VCOs, by means of current steering, have wide tuning ranges starting from less than 20-MHz up to 930-MHz and 1.22-GHz for the single-ended and differential ring VCOs respectively.  $K_{VCO}$  is quite high due to the large frequency tuning ranges with values of 210-MHz/mA and 325-MHz/mA for the two VCOs.

Power consumption is lower in the single-ended implementation. The VCO consumes only 7-mW compared to 17-mW in the differential one. The single-ended CMOS output stage is however more power hungry: it requires 45-mW which is 9-mW more than the differential CML output stage, and delivered only 25-mW to a  $50\text{-}\Omega$  load.

## V. LAYOUT CONSIDERATIONS

The chip layout is optimized for testing by making output pads of the same type on the same side of the chip. This speeds up testing and reduces possible errors that could be made since the chip needs only be translated along the x-

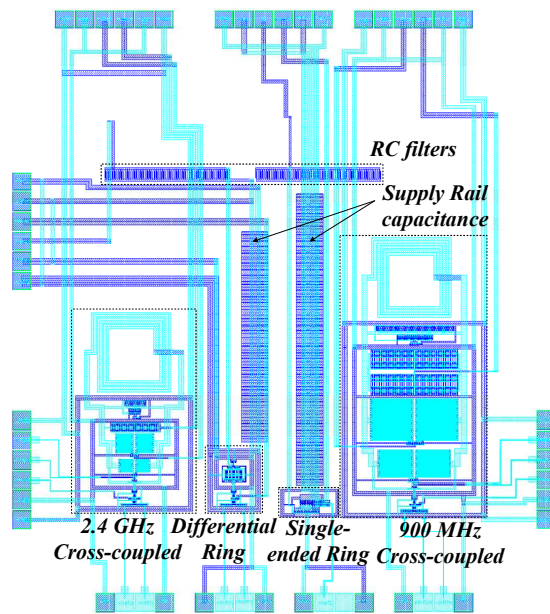


Fig. 10. Layout of the complete PROMIKRON testchip.

or y-axis to move from one transmitter structure to the next without reconnecting different probes or changing the inputs.

## VI. CONCLUSION

A test-chip consisting of four transmitter circuits was implemented on  $0.5\text{-}\mu\text{m}$  gate-array technology to investigate how RFID tags could be realized using the technology. The proposed transmitters feature simple design with direct baseband modulation through varactors or ASK modulation by use of current steering. Frequency tune was implemented in both discrete and continuous form to achieve tuning ratios of at least 35%. With 5-V supply voltage, power consumption of the VCOs varied from 7-mW up to 60-mW. The spectral purity in the cross-coupled VCOs was found to be much better than the ring VCOs.

## REFERENCES

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