Design of a Viterbi Equalizer Circuit for Data Rates up to 43 Gb/s

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***Abstract* – A chip design for a 43 Gb/s Viterbi equalizer which can be applied in optical communications is presented. The circuit is designed and fabricated in a standard 90 nm CMOS technology with a seven metal layer stack. The internal Viterbi processing is 32 times parallelized using a sliding window decoding architecture at a clock frequency of 1.34 GHz. The circuit processes incoming samples with a resolution of 3 bit. The resolution of the internal branch metrics is 6 bit. The simulated power dissipation is 2.6 W at a supply voltage of 1 V leading to 16.5 Gb/(W·s) which is a 50 times improvement compared to [1]. The chip size is 4.08 mm x 1.40 mm containing almost 500k transistors. The presented circuit is the world first Viterbi equalizer for such a high bit-rate in any technology.**

Introduction

The bit rate in current metro- and long-haul networks is 10 Gb/s and first 40 Gb/s links are under deployment. At these bit rates the signal distortions resulting from chromatic dispersion (CD) and time variant polarization-mode dispersion (PMD) are severe. Commercial equalizers are available for 10 Gb/s operation [2] and first prototypes for 40 Gb/s have been reported using analog filters. In [3] it is shown that the Maximum likelihood sequence estimation (MLSE) is the best equalization method for all possible impairments. The realization of the Viterbi algorithm which is a special realization of MLSE with less computing complexity in hardware is a challenge at these high bit-rates. Figure 1 shows an optical communication system with a Viterbi equalizer. This paper presents a Viterbi equalizer circuit for a 40 Gb/s optical receiver.

System Design

The circuit uses the parallelized decoding concept "Sliding Block Viterbi Decoder" (SBVD) [1] because a serial and recursive structure of the speed limiting add-compare-select (ACS) operation is not feasible in any technology at a clock frequency of 43 GHz.

A shown in figure 2 for shortest throughput delay time a new parallel architecture with four identical systolic block decoders (SBD) (figure 3) instead of one large SBD is proposed. This results in a four times shorter throughput delay time and lower hardware complexity. The main building blocks of each SBD are: branch metric unit (BMU), add-compare-select unit (ACSU) and trace back unit (TBU). CML demultiplexers and multiplexers are used for deserialisation and serialisation.

Circuit Design

The BMU is realized by 384 SRAM cells that allow on-line updating of the metrics during equalization. The ACSU consists of two 8 bit adders, a digital comparator and a multiplexer which selects the lower sum of the two adders. The ACSU is realized by Ripple Carry Adders (RCA) because the comparison of the sums can be done simultaneously with the add operation. The RCA is very efficient with respect to chip area and power consumption. The ACSU architecture including the critical path is depicted in figure 4. A four way multiplexer in the TBU chooses the correct decision of the four states of the trellis.

Simulation results

A worst case delay of the ACSU respectively RCA occurs if most of the gates on the critical paths are switching. The simulated delay considers two ACSUs in series with the setup- and clock-to-output delays of the flip-flop stages. By applying typical transistor and typical parasitic parameters the worst case delay is 614 ps that is lower than the internal clock period of 747 ps. The simulations are done on system level using a spreadsheet software and VHDL. The simulations are verified on transistor level using the digital "Ultrasim"-simulator which show the same result as on VHDL-level. This demonstrates the feasibility of the presented architecture for the targeted data rate. The relative figure of merit can be quantified by throughput per unit power which is equal to 16.5 Gb/(W·s). The circuit is fabricated and the experimental setup for measurements is in preparation and results will be reported soon.

Conclusion

In this paper a circuit design for a Viterbi equalizer with a new four times parallelized SBD architecture is presented. To the best of the author's knowledge this 43 Gb/s Viterbi equalizer (figure 5) is the world first with superior characteristics: 16.5 Gb/(W·s) throughput per unit power, 352 GOPS/s and 7.5 Gb/(s·mm^2) throughput per unit area (table 1).

[1] Peter J. Black and Teresa H.-Y. Meng, "A 1-Gb/s, Four-State, Sliding Block Viterbi Decoder," IEEE Journal of Solid-State Circuits, vol. 32, no. 6, pp. 797–805, June 1997.

[2] http://www.coreoptics.com/product/ic_10g_dec.php

[3] C. Fludger, et al., "Enabling Open Tolerant Networks," ECOC Workshop, 2005.

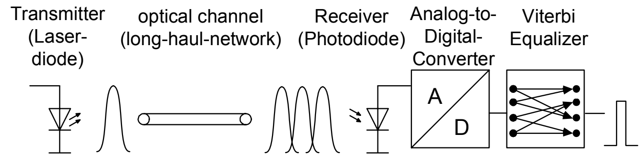

Figure 1: Optical communication link.

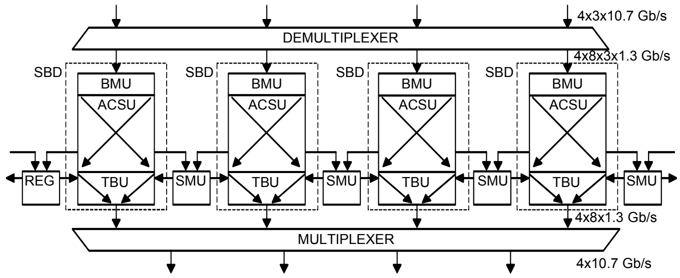

Figure 2: Chip architecture.

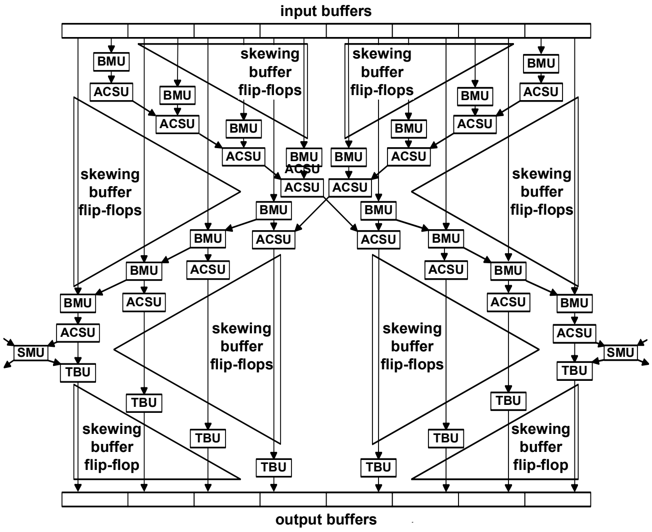

Figure 3: Block diagram of one of four systolic block decoders (SBD).

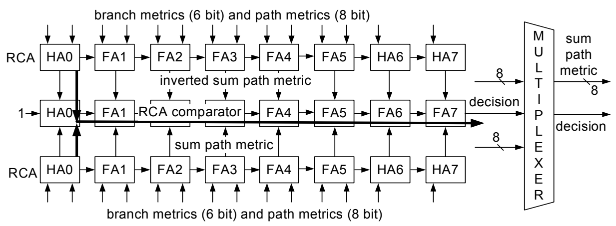

Figure 4: Block diagram of an add-compare-select unit (ACSU)

Table 1: Viterbi equalizer summary

Total power dissipation	2.6 W for 43 Gb/s
Power dissipation of DSP	1 W
Supply voltage	1 V
Chip size	4.08 mm x 1.40 mm
Count of transistors	almost 500.000
Parallelization	32
Number of ACSUs	256
Internal clock frequency	1.34 GHz
Throughput per unit power	16.5 Gb/(W·s)
Computing power	352 GOPS/s
Throughput per unit area	7.5 Gb/(s·mm^2)
Resolution of incoming symbols	3 bit
Resolution of metrics	6 bit
ACSU worst case delay	614 ps
Targeted bit error rate	10^{-3}

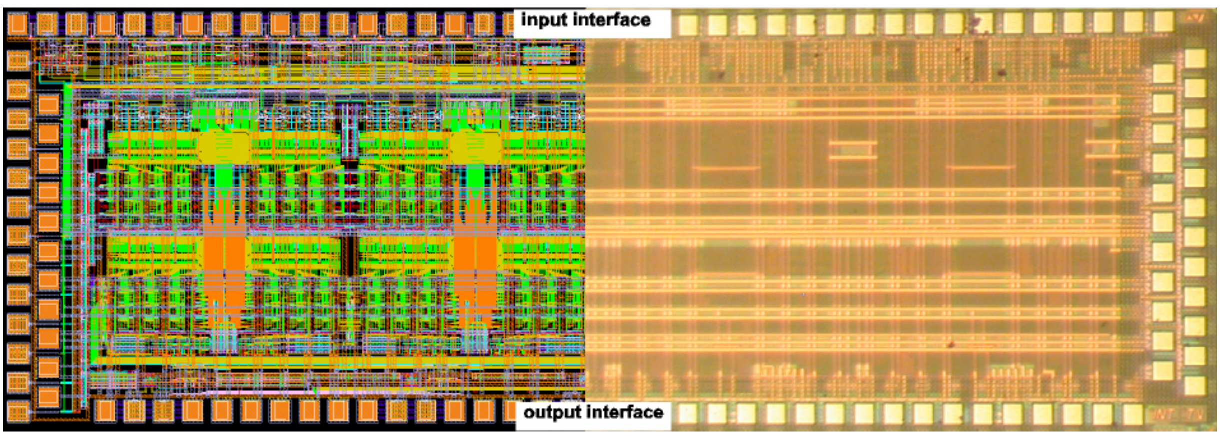

Figure 5: Layout and Chip Photograph of the fabricated 43 Gb/s Viterbi equalizer in a CMOS 90 nm technology.

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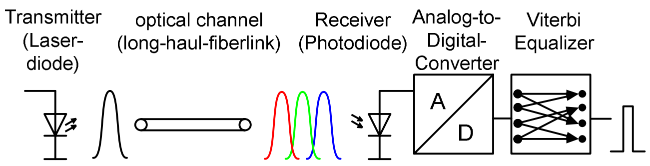
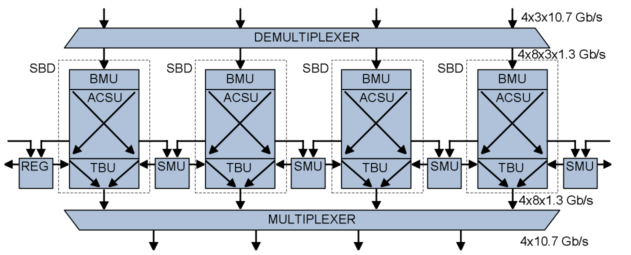
1 Optical Communication Link



Received signal suffers from
- Chromatic Dispersion (CD),
- Polarization-Mode Dispersion (PMD) (time variant).

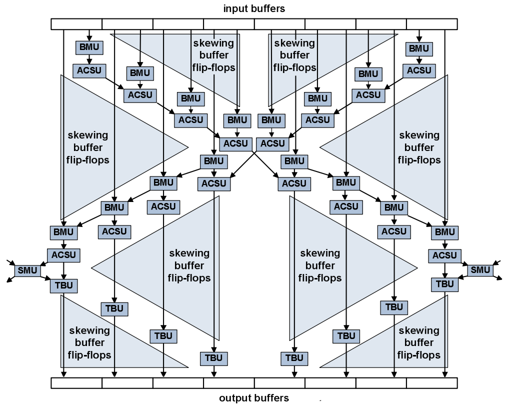
Solution:
- Maximum likelihood sequence estimation (MLSE) is the best equalization method for all impairments.
- Viterbi algorithm is a special realization of MLSE with less computing complexity and can be applied for equalization.
- The channel is modeled by two taps. Thus Viterbi decoding is done along a four state trellis to reduce the intersymbol interference.

2 Chip Architecture



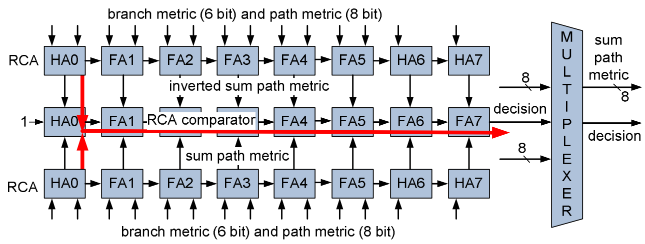
- Sliding block decoding (SBD) concept.
- Parallel architecture to reduce the throughput delay by the factor of four.
- Simultaneous equalization of 32 input symbols of 3 bit each at a clock frequency of 1.34 GHz.
- Demultiplexer and multiplexer are realized using CML.
- Digital signal processing (Viterbi equalization) is done in CMOS.

3 One of four Sliding Block Decoder



- Simultaneous forward and backward processing of the incoming data reduces the throughput delay by the factor of two.
- Branch-Metric Unit (BMU) is realized by 384 SRAM cells that allow on-line updating during equalization due to the time variant PMD.
- Trace-Back Unit (TBU) consists out of a fourway multiplexer which chooses the correct decision of the four state trellis.

4 Add-Compare-Select Unit (ACSU)

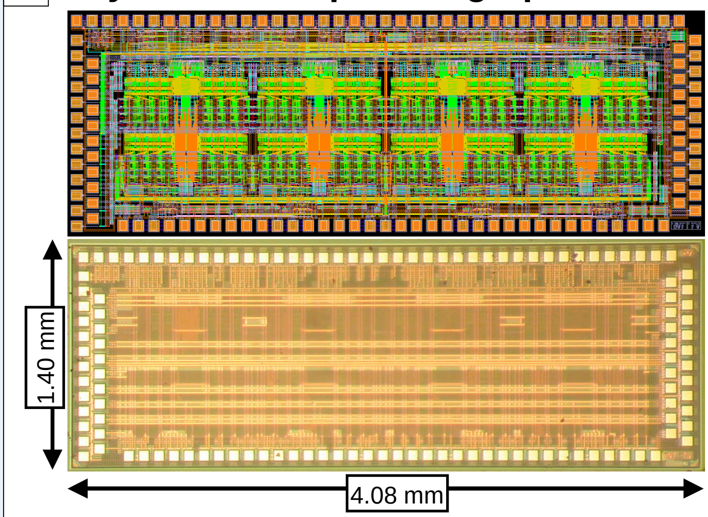


- ACSU consists of two 8 bit Ripple Carry Adders (RCA), a digital comparator and a multiplexer.
- RCA is very efficient with respect to chip area and power consumption.
- Add operation and comparison can be done simultaneously.
- Worst case delay along the critical path depicted in red for one ACSU is only 614 ps.

5 Viterbi Equalizer Summary

Technology	ST 90 nm CMOS GP
Total power dissipation	2.6 W for 43 Gb/s
Power dissipation of DSP	1 W
Supply voltage	1 V
Chip size	4.08 mm x 1.40 mm = 5.7 mm^2
Count of transistors	almost 500.000
Parallelization	32
Number of ACSUs	256
Internal clock frequency	1.34 GHz
Throughput per unit power	16.5 Gb/(W·s)
Computing power	352 GOPS/s
Throughput per unit area	7.5 Gb/(s·mm^2)
Resolution of incoming symbols	3 bit
Resolution of branch metrics	6 bit
ACSU worst case delay	614 ps
Targeted bit error rate	10^{-3}

6 Layout and Chip Photograph



World first Viterbi equalizer for 43 Gb/s with superior characteristics
- 16.5 Gb/(W·s) throughput per unit power
- 352 GOPS/s
- 7.5 Gb/(s·mm^2) throughput per unit area

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