25 GS/s 6-bit Pseudo Segmented Current Steering DAC in 90 nm CMOS

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***Abstract*—This paper describes the design of a 25 GS/s 6-bit current steering digital-to-analog converter (DAC). The DAC is implemented with a pseudo-segmented and twofold time-interleaved architecture using a commercial 90 nm CMOS process. Layout level simulation results indicate 4.96 effective number of bit (ENOB) for a sinusoidal input of 12.3 GHz at a sampling frequency of 25 GHz with a power dissipation of 2.7 W. The chip design is finished and submitted for fabrication.**

I. Introduction And Architecture

The main application for high-speed DACs are 40-100 Gbit/s optical core and metro networks that use advanced digital modulation formats.

DAC architectures can be classified as binary, unary and segmented architectures. Binary architectures are used to save power and to reduce chip area whereas unary architectures show better static and dynamic performance. Linearity is improved, monotonicity is guranteed and glitch power is decreased. Segmented architectures allow for trade-off between complexity and performance.

This circuit is implemented with a pseudo-segmented architecture [1]. No binary-to-thermometer decoder is used to control the unary weighted current sources. Flip-flop stages with different weight, i.e. different driving capabilities are used instead to control the unary and binary current sources.

Fig. 1 shows the twofold time-interleaved architecture of the DAC [2]. It consists of two identical 6-bit DACs working on the positive and the negative clock edge. Thus the clock frequency of the DACs can be reduced to half the sampling frequency.

The 6-bit DACs consist of a clock distribution network, a input synchronization unit, data buffers, binary and unary weighted cascode current sources and switches. Due to the maximum clock frequency of 12.5 GHz the clock buffers in the distribution network are peaked with inductors. The clock distribution network feeds the input synchronization units and the current switches. The input synchronization units allow to sample the digital inputs at two phases (0°,180°). Data buffers are used to regenerate and to shift the voltage levels according to the requirements of the current switches. Cascode current sources support high output impendance and directly drive a 50 Ω termination. The differential analog output voltage swing is tunable up to ±500 mV.

The “Synchronization Evaluation Logic Unit” (“SELU”) is implemented to support the off-chip synchronization of the high-speed digital input signals. The “SELU” and the input synchronization units are controlled via programmable registers. Fig. 2 shows the block diagramm of the “SELU”. Two adjacent digital input signals are XOR-combined to detect the synchronization of the channels. Adjacent channels can be chosen by a select stage and the control registers. The chosen XOR-combined output pulses are stretched for off-chip detection.

II. Layout

Fig. 3 shows the floorplan of the DAC core. The time-interleaving technique results in a complete symmetrical layout of the DAC core. The layout of the switches and current sources are optimized to avoid interleaved channel mismatch. Fig. 4 shows the layout of the entire DAC.

III. Simulation Results And Conclusion

Simulations are made on transistor-level in a 90 nm standard CMOS technology at a -2.5 V supply voltage. A reduction of the supply voltage to -2.0 V is possible. Resimulations are based on typical layout parasitics. To determine the ENOB, a digital sine tone is applied to the input of the DAC. The SNDR and the resulting DAC-specific ENOB is calculated from the Fourier transform of the analog DAC output signal. Fig. 5 shows the ENOB curves for a sampling frequency of 25 GHz. The ENOB curve of an ideal DAC with a staircase-like output signal is included in the diagram to compare the results. The complete DAC has a power consumption of 2.7 W whereas the DAC core consumes only 2.3 W. Table 1 summarizes the resimulated DAC performances.

References

[1] P. Palmers et al., “A 130 nm CMOS 6-bit Full Nyquist 3 GS/s DAC”, IEEE Asian Solid-State Circuits Conference, November 12-14 2007, Jeju, Korea.

[2] M. Grözing et al., “High-Speed ADC Building Blocks in 90 nm CMOS”, Joint Symposium on Opto- and Microelectronic Devices and Circuits SODC September 02-08 2006, Duisburg, Germany.

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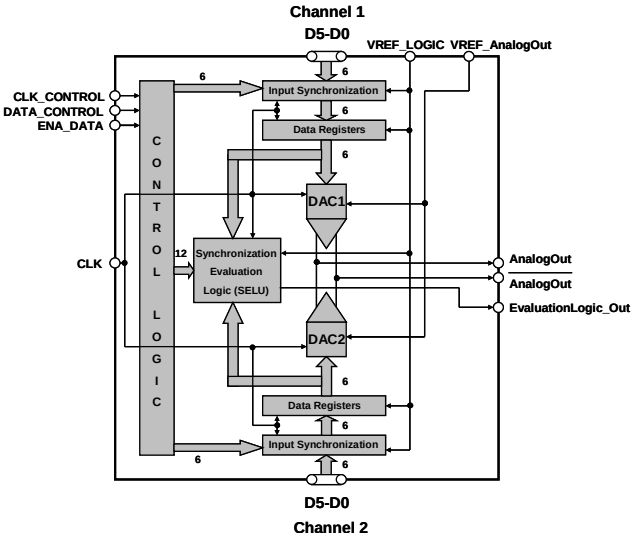

Figure 1. Twofold time-interleaved architecture of the 6-bit DAC.

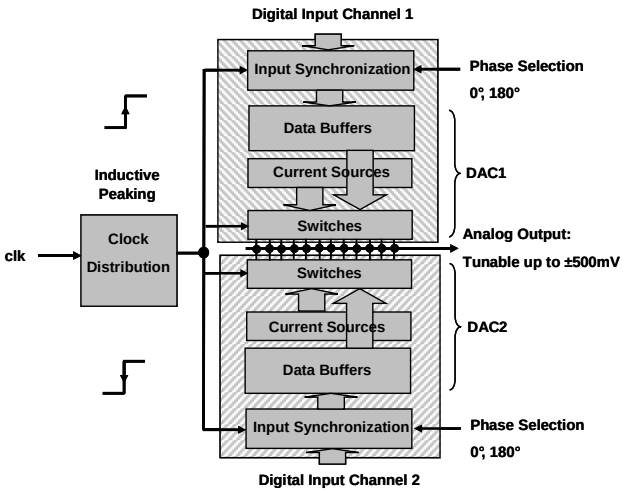

Figure 3. Floorplan of the 6-bit DAC core.

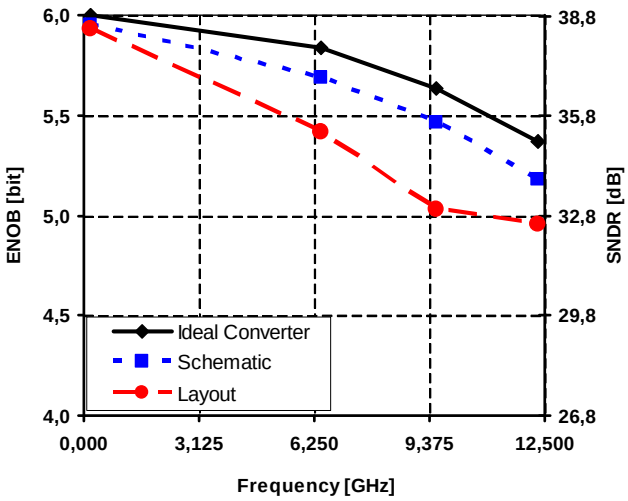

Figure 5. ENOB curves for a sampling frequency of 25 GHz.

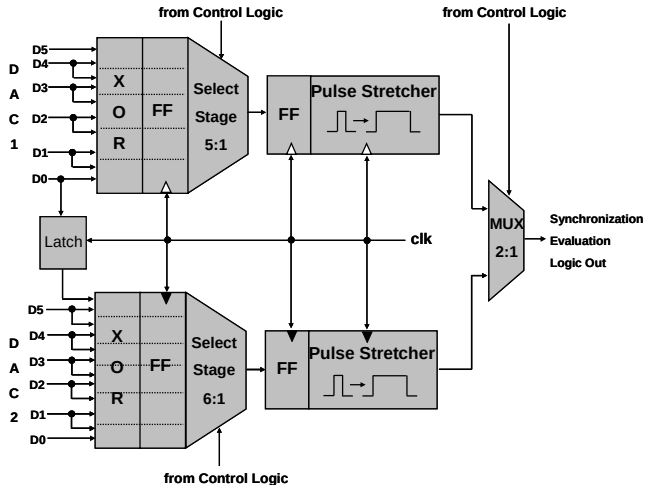

Figure 2. Synchronization Evaluation Logic Unit ("SELU").

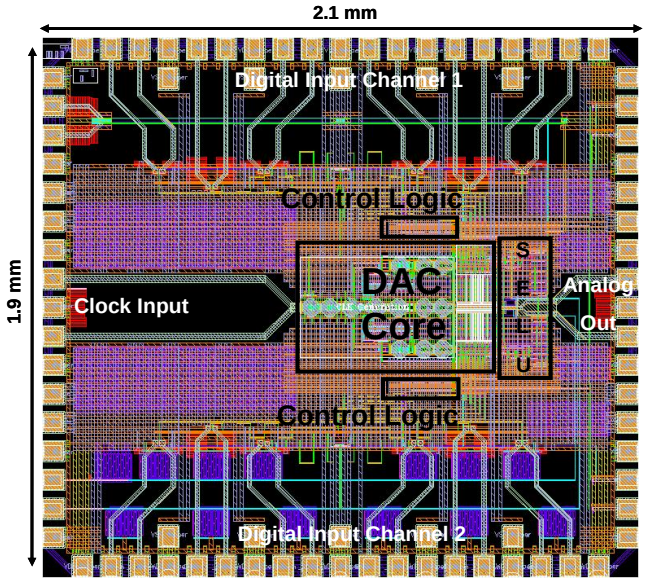

Figure 4. Layout of the entire 6-bit DAC.

Process:	90 nm CMOS GP
Nominal Resolution:	6 bit
Sampling Rate:	0 ... 25 GS/s
Effective Resolution @ 25 GS/s: @ DC (195.312 MHz) @ Nyquist (12.304 GHz)	 5.93 bit 4.96 bit
Power consumption: DAC core @ -2.5 / -2.0 V: DAC chip @ -2.5 / -2.0 V:	 2.3 W / 1.7 W 2.7 W / 2.2 W
Die area with pads / core area:	4 mm^2 / 0.28 mm^2
Supply Voltages:	VDD: 0 V VSS: -2 ... -2.5V

Table 1. Simulation results based on layout with extracted parasitics.