Design of a 25 GS/s 6-bit Flash-ADC in 90 nm CMOS technology

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Abstract—**A twofold time-interleaved interpolating Flash-Analog-to-Digital Converter (ADC) with an effective resolution greater than 5.3 bit for low frequencies and more than 3.3 bit up to Nyquist-frequency at 25 GS/s is presented. The power consumption is 2.75 W and it includes a new calibration technique. The ADC is designed in a 90 nm CMOS process and is submitted for fabrication.**

I. Architecture

The 6-bit ADC is based on 3-bit coarse quantization combined with three stages of active interpolation [1]. The track & hold operations are based on transfer-gates with input-output compensation [2] to avoid clock-feedthrough. Each ADC channel has its own differential reference ladder to minimize crosstalk between the two ADCs and to allow for individual mismatch compensation.

Compensation of mismatch in the coarse quantization network is implemented by shiftable reference voltages. The voltage shifts can be controlled by a separate register. The coarse mismatch compensation improves the linearity and thus the signal-to-noise-and-distortion ratio (SNDR) and the effective number of bits (ENOB) of the ADC.

Fig. 1 shows the concept of a single ADC channel with a sampling rate up to 12.5 GS/s. The interpolation network is built up symmetrically. It is terminated at both ends by interpolation-amplifier-dummies to provide for constant load impedance. The active interpolation amplifiers (AIA) and the amplifiers in the interpolation network are optimized with respect to maximized linearity and minimized input capacitance.

The final decision takes place in the flip-flops (FF) after the analog part of the circuit. The thermometer-to-binary-decoder is an improved version of the multiplexer-based decoder in [3]. It is robust against bubble-errors which were estimated to arise only singularly by monte-carlo simulations.

The final circuit implementation is shown in the block diagram of Fig. 2. It shows the master and slave configuration of the twofold time-interleaved structure. There is an on-chip pseudo random bit sequence generator (PRBS) to allow for off-chip synchronization of the 12 high-speed digital output lines. The register controls the activation of the PRBS, the output signal and the calibration circuit.

II. Layout

The layout of the converter is shown in Fig. 3. The chip has a total size of 2.1 x 1.9 mm^2. It is pad-limited with a core size of only 500 x 600 μm^2. The analog input- and the clock-signals are routed to the middle of the chip with 50 Ω lines and then distributed to the two single-ADCs. Fig. 3 also shows the placement of the other components of the circuit. The PRBS generator, the thermometer-to-binary-decoder and the reference ladder are included within the core area.

III. Simulation Results and Conclusion

In standard operation mode the circuit consumes 2.75 W. The power dissipation is nearly constant with clock frequency due to a differential CML-structure. The ADC core consumes only 2 W.

Fig. 4 shows the dynamic performance of the converter, namely SNDR and ENOB over input signal frequency. Results are shown for simulations on schematic level and on extracted layout level with parasitics, each for sampling rates of 25 GS/s and 16.7 GS/s.

The resolution is more than 5.3 bit for low frequencies in all simulations. Furthermore the plot shows that operation for higher signal frequencies, e.g. at 25 GS/s tends to a higher decrease of resolution than it does for 16.7 GS/s. This is due to the available settling time in the interpolation network that decreases with increasing sampling frequency. Table 5 summarizes the performance of the ADC.

References:

[1] R. van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd Ed., 2003.

[2] M. Grözing, M. Berroth, "High Speed ADC Building Blocks in 90 nm CMOS", 4th Joint Symposium on Opto- and Microelectronics Devices and Circuits – SODC 2006, Duisburg, Sept. 2006.

[3] Erik Sall and Mark Vesterbacka, "Thermometer-to-Binary Decoders for Flash Analog-to-Digital Converters", Department of Electrical Engineering, Linkoping University, Sweden, 2007
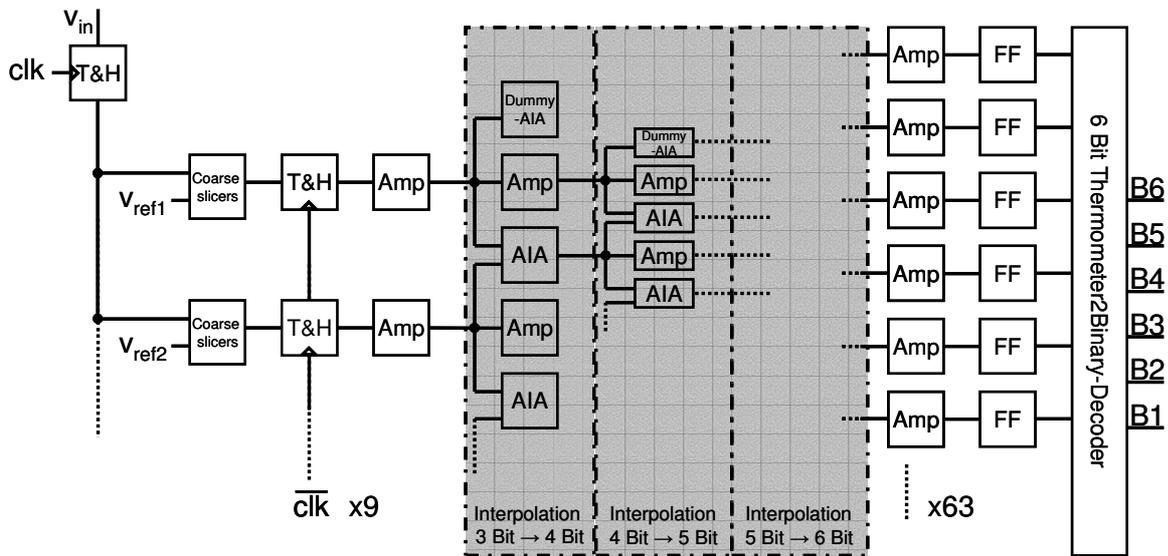
Figure 1. Concept of a single ADC channel with interpolation network and active interpolation amplifiers (AIA)
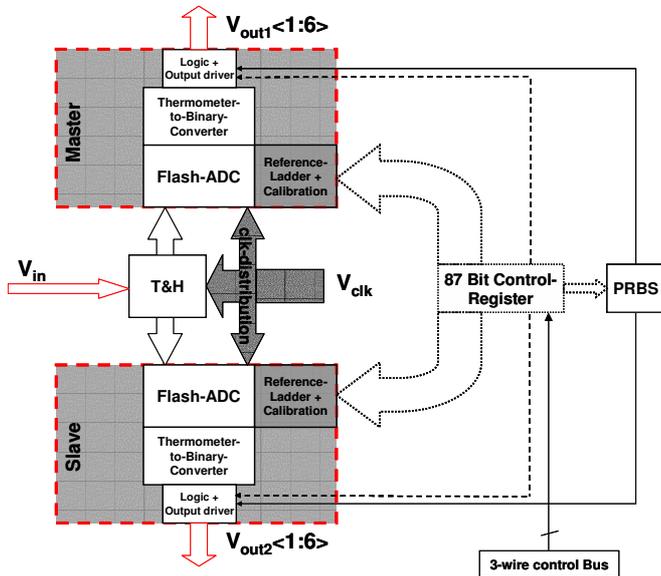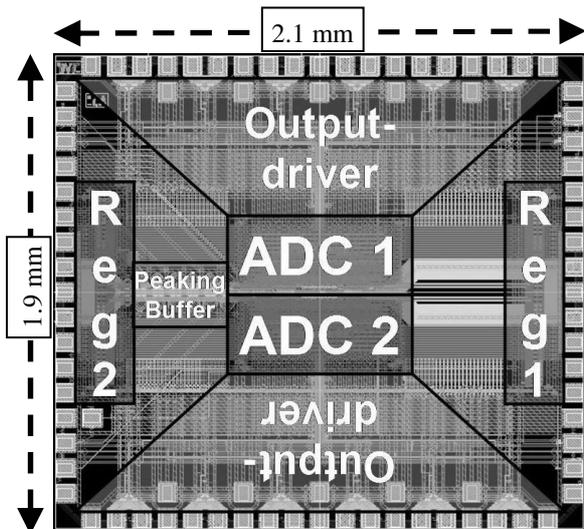

Figure 2. Block diagram of the whole ADC
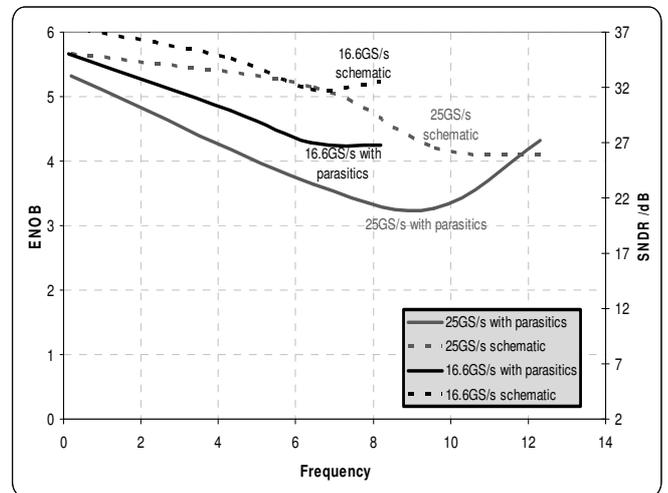

Figure 3. Layout of the 6-bit ADC-chip

Figure 4. ENOB for 25GS/s and 16.7GS/s simulated for schematic and resimulated with parasitics

Technology	ST 90 nm CMOS GP
Concept	Flash + Active Interpolation
Chip-/Core-Size	2.1 x 1.9 mm^2/0.6 x 0.5 mm^2
Nominal resolution	6 bit
Power dissipation chip/core	2.7 W / 2.0 W
Sampling rate	0 .. 25 GS/s
ENOB 25GS/s @ 0.19 GHz / 6.4 GHz	5.3 / 3.7
ENOB 16.7GS/s @ 0.13 GHz / 6.4 GHz	5.6 / 4.3
Supply Voltages (nominal)	1) VDD 0V; VSS -1.25 V 2) VDD_overdrive 0.5 V; VSS -1.25 V

Table1. ADC-specifications and simulation results