

Design of a Quadrature Clock Conditioning Circuit in 90-nm CMOS Technology

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Abstract—This paper presents the operation and problems of the conventional clock conditioning circuits. A modified design is proposed to eliminate these problems and to merge two conditioning circuits together. This is to adjust and maintain two output signal properties actively during circuit operation for 4-phase 10 GHz single-ended clock signals. It is desired to have an exact 50% duty-cycle for each signal and a 90° phase difference between them. Simulation results in 90-nm CMOS technology are provided showing low output jitter.

Index Terms—Clocks, CMOS Integrated Circuits, Duty-Cycle Control, Feedback Circuits, Phase Control.

I. INTRODUCTION

IN sequential systems, a precise clock signal is required for optimum operating conditions. For example, a 40-Gs/s four time-interleaved flash ADC requires 4-phase clock signals, each having an exact 50% duty-cycle (the ratio of the pulse width to the period time) and a 90° phase difference between them [1]. Both signal properties have to be maintained during circuit operation under all operating conditions.

A high-speed current mode logic (CML) clock divider circuit (prescaler with division ratio of 2) like those introduced in [2] is used to provide the 10 GHz 4-phase single-ended clock signals with the required properties from a 20 GHz differential input clock signal. A CML-to-CMOS circuit is used to convert the CML output levels of the CML clock divider to the binary CMOS level periodic clock signals. Finally, CMOS drivers are used to buffer the clock signals to be distributed throughout the chip. In practice, the quadrature clock circuit and the drivers used above exhibit variations due to mismatch, process and temperature variations. Though, a small error in the clock signals may actually cause a significant impact on the system performance. Therefore, a feedback correction loop is needed to compensate and actively adjust these static or dynamic variations to provide an output signal with defined phase difference and duty-cycle.

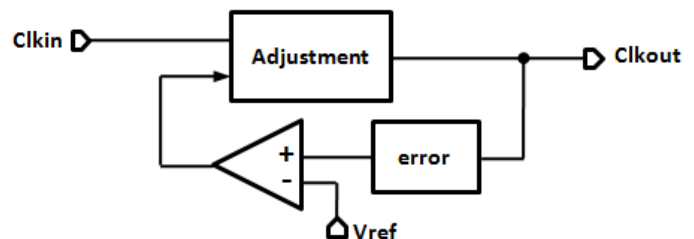


Fig. 1. Block diagram of the conventional clock conditioning circuit.

This paper presents the conventional conditioning circuits in Section-II. The modified design and discussion of its operation are provided in Section-III. Simulation results are presented in Section-IV. Finally, conclusions are given in Section-V.

II. CONVENTIONAL CONDITIONING CIRCUIT

Fig. 1 shows the block diagram of the conventional clock conditioning circuit that is composed of three main blocks; an adjustment circuit to adjust the variations in the single-ended clock signal depending on the control signal, an error measurement circuit to measure the desired output property (duty-cycle) of the output clock signal and a comparator circuit to generate a feedback control signal depending on the difference between the actual measured value and the reference value [3-4]. Schematic simulations show that this feedback system has the desired output response, where the measured voltage signal smoothly oscillates around the reference value in steady state. However, several problems arise in applications.

First, as shown in the block diagram, a constant reference signal is assumed to be available and stable during circuit operation. Though, any variations in the reference signal due to process variations will cause an error in the output signal. Second, the comparator circuit is implemented using a high-gain differential amplifier with an output stage to have rail-to-rail output voltage swing. For any differential amplifier there is a defined input common-mode range, to have all transistors working in the saturation region. A level shifter circuit is used to shift the dc level of the measured value to adjust it within

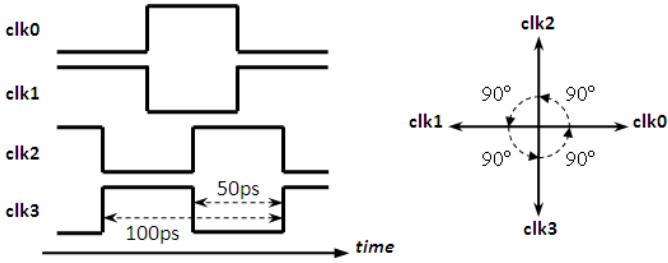


Fig. 2. Ideal 10 GHz 4-phase single-ended clock signals.

the allowed range. However, any process variations in the level shifter introduce errors to the output signal. Third, as transistors determine the rise and the fall times, variations at the transistor parameters result in duty-cycle variations. Therefore, a conditioning circuit that eliminates the above problems and provides further benefits and accurate output conditions is proposed in the next section.

III. THE QUADRATURE CLOCK CONDITIONING CIRCUIT

Fig. 2 shows the ideal 4-phase single ended clock signals, where each signal exhibits an exact 50% duty-cycle. The required phase differences between the signals are illustrated also in Fig. 2.

Fig. 3 shows the block diagram of the proposed design that is composed of a duty-cycle control loop for each differential clock signal and a phase control loop between the two differential clock signals. First the duty-cycle control loop includes two low-pass filters, comparator and a CML duty-cycle adjustment circuit. The low-pass filter is a circuit that measures the average value of each complementary signal. The comparator generates a feedback control signal depending on the difference between the two measured values. The CML duty-cycle adjustment circuit adjusts the duty-cycle of the differential clock depending on the feedback control signal. Second, the phase control loop includes a phase difference measurement block (PDM), comparator and an adjustable delay circuit placed on each differential clock signal. The role of the PDM is to generate two output signals that will have equal amplitudes if and only if the phase difference between the differential signals is exactly 90° as desired. The comparator block detects the difference between those two signals and generates a feedback differential control signal. Depending on the value of the control signal, the phase difference between the differential clock signals is reduced or extended. This is achieved by increasing the delay of the first differential clock signal and decreasing the delay of the second one to reduce the phase difference and vice-versa. Finally, CML-to-CMOS and CMOS-buffer blocks are placed at the output. This is to convert the CML output levels of the adjustment circuits to the desired CMOS clock signal levels and to buffer the clock signals to be distributed throughout the chip. A comparator circuit with an output stage is used to implement the CML-to-CMOS block to generate the necessary

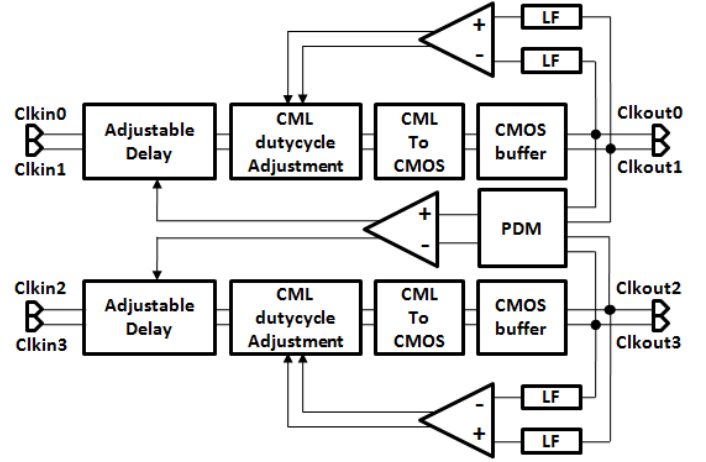


Fig. 3. Block diagram of the quadrature clock conditioning circuit.

output rail-to-rail voltage swing. The CMOS-buffer includes a chain of inverters to drive a large capacitive load and it is proposed to add a cross-coupled inverter pair between each complementary signal to ensure and maintain a 180° phase shift between them.

The operation of the duty-cycle control loop is to compare the average values of the two complementary signals with each others as shown in Fig. 3. Any difference is detected by the comparator and generates a feedback control signal that reduces this difference. This is because two complementary signals will have the same average value if and only if the duty-cycle of both signals is exactly 50%. Therefore, as the system reduces the difference between the two measured average values, the duty-cycle of the clock signals will approach the desired 50%.

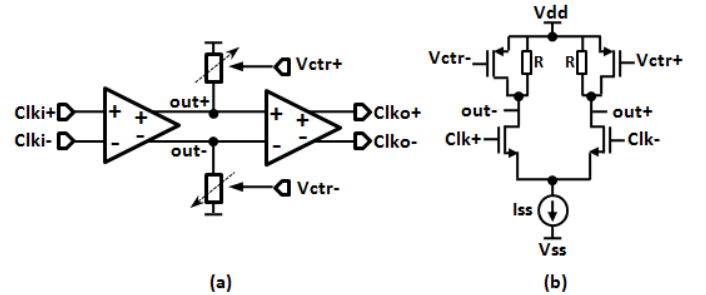


Fig. 4. (a) Block diagram of the CML duty-cycle adjustment circuit, (b) Schematic of the input CML-buffer with additional parallel PMOS loads.

The idea of a high-speed duty-cycle control circuit reported in [5] is used to implement the CML duty-cycle adjustment circuit. There are two modifications proposed. This circuit includes two CML-buffers and programmable loads as shown in Fig. 4(a). The idea of this method is to buffer the clock signals using the first CML-buffer then changing the dc bias level of one of the complementary signals and then finally restores the initial signal levels at the final output using the second CML-buffer. The first modification proposed is to increase the dc bias level of the first complementary signal and decrease the dc bias level for the second signal as well or

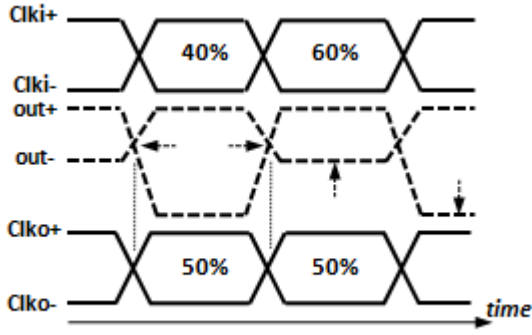


Fig. 5. Signal waveforms for the CML duty-cycle adjustment circuit.

vice-versa. This is to extend the tuning range of the adjustment circuit and to achieve symmetry in the design to minimize mismatching problems. The second modification is that the programmable load is implemented using a PMOS transistor parallel to the resistive load of the first CML-buffer as shown in Fig. 4(b). This is done instead of using multi-bit input programmable load as presented in [5]. With reference to the waveforms shown in Fig. 5, the operation of the CML duty-cycle adjustment circuit is illustrated. It shows how the duty-cycle will reach the desired 50% at the output from a 40% input duty-cycle.

As mentioned briefly before, the operation of the phase control loop is to compare two measured values that are equal only when the phase difference between the two differential clock signals is 90° . Therefore, the feedback control signals reduce the difference between these measured values by extending or reducing the phase difference between the two differential clock signals. For example, the phase difference is reduced by increasing the delay of the first differential clock signal and decreasing the delay of the second signal using the adjustable delay circuits. Several methods can be applied to implement the adjustable delay circuit. For example, the same circuit as the CML duty-cycle adjustment circuit shown in Fig. 4(a) and Fig. 4(b) can be used, the only modification is to connect the gates of both PMOS load transistors to the same control signal. Another modification proposed is to replace each PMOS load transistor by a three-terminal varactor.

Referring to Fig. 6, the idea of the proposed method used to generate the two measured values is illustrated in the phase plane. Where $\Delta\varphi_1$ is the phase difference between the clock signals Clk2 and Clk0, $\Delta\varphi_2$ is the phase difference between the clock signals Clk1 and Clk2. Therefore, $\Delta\varphi_1$ will be equal to $\Delta\varphi_2$ if and only if the phase differences between the signals are exactly as desired (Fig. 2). Thus, $\Delta\varphi_1$ and $\Delta\varphi_2$ are the two measured values which are compared. Linear phase detectors (LPD) will be used to generate these measured values as shown in Fig. 7. Noting that the same comparison described above is used but for differential signals instead of single-ended signals. The LPD can be implemented using the basic Gilbert cell and a low-pass filter to get the average value of the output signal [6].

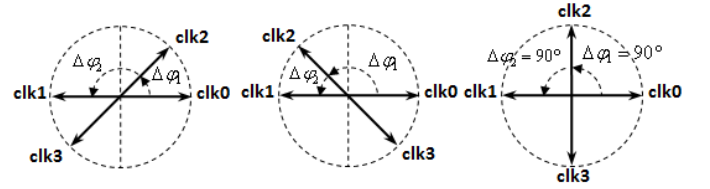


Fig. 6. Three possible cases for the phase differences between the four single-ended clock signals.

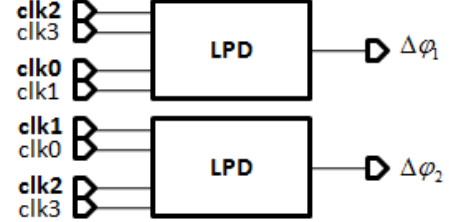


Fig. 7. Implementation of the phase difference measurement block (PDM).

By comparing the proposed design to the conventional one, the problems stated in Section-II are eliminated. First, no reference voltages are used in the circuit. Second, the comparators are designed to have the proper common-mode range to avoid using level shifters in the design. Third, only one type transistor (p-type) is used for both adjustment circuits to adjust the signals. This will ensure that the rise and the fall times of the output signals will be affected similarly if any process variations exist, resulting in no change in the duty-cycle. A further benefit to the present design is that all blocks of the control loops are implemented using differential circuits which increase the noise immunity of the system. Finally, two conditioning circuits are merged without making any loop depending on the response of any other loop to avoid accumulation of errors. Therefore, the proposed design is more reliable and practical.

IV. SIMULATION RESULTS

Simulations are performed using the Spectre simulator in a 90-nm CMOS technology. Two power supplies are used in the design, a 1V and a 2.5V for CMOS and CML blocks respectively. A higher supply voltage is used for the CML blocks to increase their input common-mode range. The input bandwidth of the CML circuits is increased by using cascoded current sources in the design.

First, typical operating conditions are used in the simulation at 27°C ambient temperature. A clock divider circuit is used to generate the 10 GHz 4-phase single-ended clock signals from a 20 GHz differential clock input signal. In steady state operation, the output duty-cycles smoothly oscillate around the desired 50% and the phase differences between the output clock signals also oscillate smoothly around the required 90° . By choosing proper time-constant values for the low-pass filters in the design, the oscillations

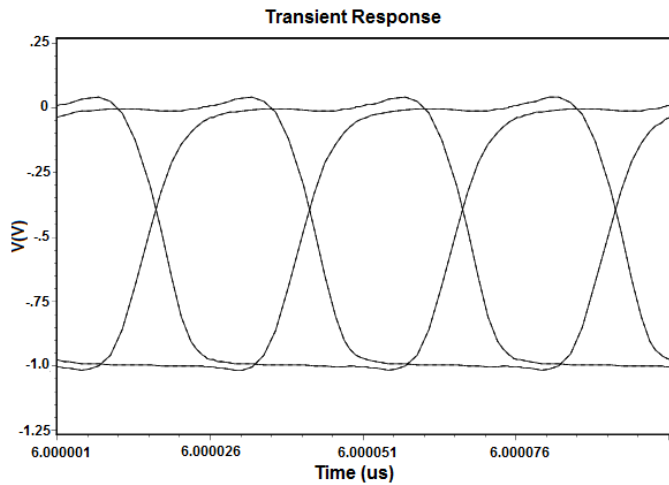


Fig. 8. The 10 GHz 4-phase single-ended output clock signals.

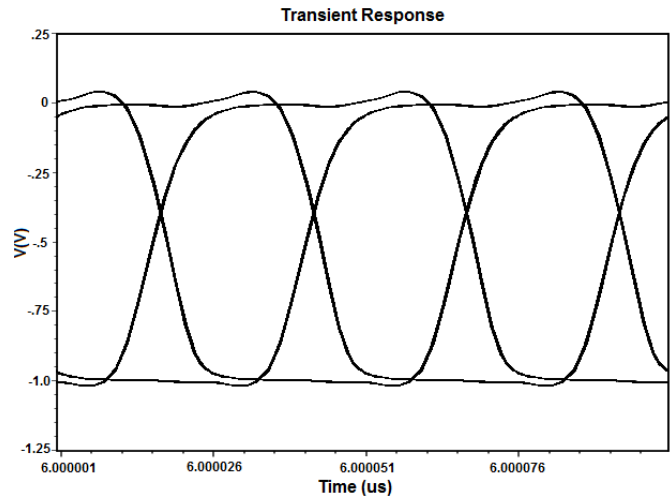


Fig. 9. Eye-diagram for the 4-phase output clock signals from 6 μ s to 8 μ s.

around the desired value and the output clock jitter can be significantly reduced. Fig. 8 shows the four output clock signals overlapping each others, where each signal has a $50\% \pm 0.2\%$ duty-cycle and the phase differences between them are $90^\circ \pm 0.3\%$. This $\pm 0.2\%$ and $\pm 0.3\%$ are the variations due to the smooth oscillations around the desired value. The eye-diagram of the output clock signals from 6 μ s to 8 μ s is shown in Fig. 9, where the peak-to-peak clock jitter is approximately 200 fs.

Second, the circuit is also tested in several non-typical operating conditions. For example, fast or slow transistor models are used instead of ideal models at high temperature of 80° C. The only change is that the circuit takes more time after start-up to reach the steady state operation.

Third, 100 iterations for the statistical Monte Carlo simulation are performed to test the circuit under process variations and mismatch conditions. All the 100 iterations achieved the desired output response.

Finally, the allowed input error range is determined by adding errors intentionally to the input. Simulation results show that $\pm 10\%$ error around the desired 50% duty-cycle and ± 5 ps around the required 25 ps delay between the signals can be adjusted successfully.

V. CONCLUSION

In this paper, a proposed quadrature clock conditioning circuit in 90-nm CMOS technology is presented. The circuit automatically adjusts 4-phase clock signals, providing a stable 50% duty-cycle for each signal and an accurate 90° phase difference between them. Simulation results show a low output jitter of 200 fs for the output clock signals with a wide input error range of $\pm 10\%$ for the duty-cycle and ± 5 ps for the delay between the signals to be corrected.

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