Concept for a 12-bit Digital Bandpass Delta-Sigma Modulator for Power Amplifier Applications

Thomas Alpert, Martin Schmidt, Ingo Dettmann, Thomas Veigel, Markus Grözing, Manfred Berroth

Institute of Electrical and Optical Communications Engineering

Universität Stuttgart

Stuttgart, Germany

***Abstract*—A digital bandpass delta-sigma modulator (BPDSM) with an SNR of 74 dB at a bandwidth of 20 MHz is proposed. A time-interleaved structure and optimized sparse-tree adders ensure a high sampling frequency and thus a high input signal frequency range. The concept is based on static CMOS gates using a commercial 65 nm process. Simulations indicate a sampling frequency up to 6.6 GHz and a signal frequency of up to 1.67 GHz.**

I. INTRODUCTION

Modern coding schemes in wireless communications have a much higher peak-to-average-power-ratio (PAPR) than those used in former standards. Though, the efficiency of the widely spread linear power amplifiers (PA) decreases rapidly with growing PAPR. A possible solution is the class-S PA concept which has already been used successfully for audio applications.

A class-S amplifier consists of a modulator, a switching-mode amplifier and a reconstruction filter [1]. In a first approach only the power amplifier is replaced by a class-S amplifier. But in long term, direct digital conversion up to the switching-mode amplifier is considered beneficial. The modified transmission chain for this case is shown in Fig. 1. The baseband signal is sampled up to the sampling frequency of the modulator and digitally mixed with the RF carrier. Then the modulator converts the low bandwidth but high resolution input signal into a noise shaped bitstream. The switching-mode amplifier, e.g. a class-D amplifier, operates only in two working points and is thus very efficient for signals with high dynamic range. Finally an analog bandpass filter removes out-of-band power from the output signal.

This article presents a concept for the BPDSM which plays a key role in a class-S amplifier. In Section II an overview of the architecture of the modulator will be given. Section III deals with arithmetic operations of the modulator, especially with the sparse tree adder and its modifications. Simulation results are discussed in Section IV. A conclusion is given in Section V.

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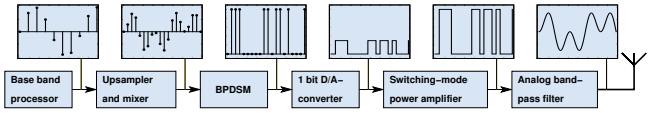

Figure 1. *Block diagram of a transmission chain with digital class-S amplifier*

II. ARCHITECTURE

A. *Model of a fourth-order bandpass delta-sigma modulator*

Fig. 2(a) shows the linear model of a fourth-order BPDSM. The output signal

$$Y = z^{-4}X + \left(1 + 2z^{-2} + z^{-4}\right)E \qquad (1)$$

consists of two parts. The part transferring the input signal X is called the signal transfer function (STF). The STF only delays the input signal. The part transferring the quantization error E is called the noise transfer function (NTF). The NTF shapes the quantization noise and removes it within the signal band having a bandstop characteristic. The notch is located at $f_s/4$. One possible digital realization is a direct conversion of the model according to Fig. 2(b). The input signal is quantized with 12 bit and internally extended to 16 bit preventing overflows. Positive and negative signal values are coded using 2K-arithmetic. Thus the extension is achieved via a multiplexer filling the upper 4 bit with zeros or ones depending on the MSB. The delay elements are realized with 16-bit registers. The 1-bit quantizer is realized as a 2-to-1 multiplexer which feeds back the positive or negative feedback value depending on the MSB. The multiplication is realized via a 1-bit left shift operation.

Two arithmetic operations have to be executed during one clock cycle. Considering e.g. the mobile standard UMTS (Universal Mobile Telecommunication System) with a downlink band at 2.14 GHz, the signal must be sampled at four times the signal frequency, i.e. $f_s = 8.56\,\text{GHz}$. Currently

there are no technologies and adders available that can support two 16 bit subtractions within one 8.56 GHz clock cycle. Another drawback is the feedback loop that prevents the use of pipelining techniques.

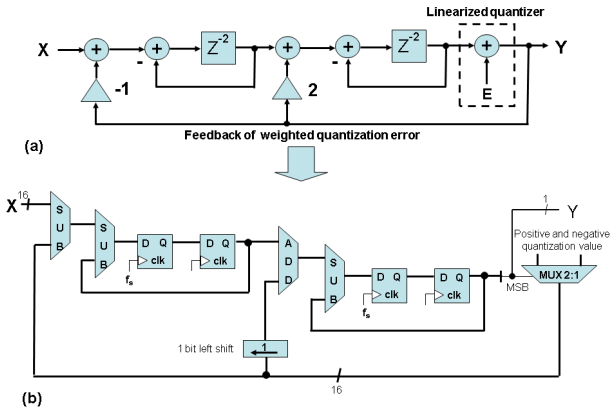

Figure 2. *a) Linear model and b) digital realization of a fourth-order BPDSM*

B. *Time-Interleaved Approach*

A possible approach to reduce the speed requirements is the time-interleaving technique [2]. A twofold time-interleaved structure can be realized. This is due to the z^{-2} delay elements (Fig. 2(a)) permitting to process the even and odd samples independently. Like in parallel structures the modulator according to Fig. 2(b) is doubled. One unit is working on the positive clock edge processing the odd data. The copy is working on the negative clock edge processing the even data. The clock frequency of the units can be reduced to $f_s/2$. A demultiplexer at the system input and a multiplexer at the system output are used to sample the input and output data with frequency f_s. Fig. 3 shows the time-interleaved architecture of the digital modulator.

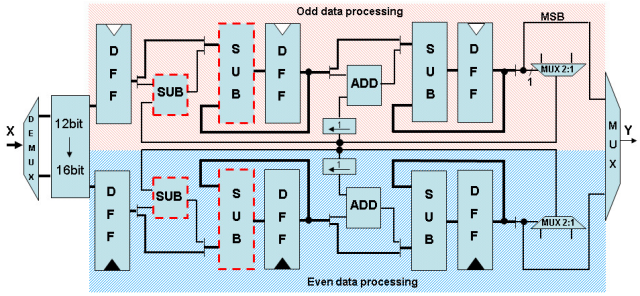

Figure 3. *Time-Interleaved architecture of the digital BPDSM*

Further improvements can be done by choosing a proper feedback value from the quantizer simplifying the first subtraction and addition of the two consecutive operations.

III. ARITHMETIC OPERATIONS

The arithmetic units play a key role in a purely digital realization. The maximum clock rate is mainly limited by the two consecutive subtractions marked in Fig. 3 with dashed lines. The first subtraction is realized by a ripple carry scheme choosing a proper feedback value from the quantizer. The second block is a 16-bit subtraction and is the most critical part. One of the fastest adding schemes is the Sparse-Tree adder presented in [3-6]. This scheme is used in a modified manner in the design.

A. *Sparse-Tree-Adder*

The Sparse-Tree adder can be classified as a hybrid-adder combining the concepts of prefix and conditional sum addition to achieve maximum speed due to reduced fan outs and wiring complexity. Fig. 4 shows the structure of the 16 bit Sparse-Tree adder.

The structure consists of three building blocks and can be separated in a critical and a noncritical section. The critical path is marked in Fig. 4 with dashed lines. In the critical section the propagate-generate block generates the propagate and generate signals from the inputs A_i and B_i:

$$P_i = A_i + B_i, \tag{2}$$

$$G_i = A_i \cdot B_i. \tag{3}$$

The block is followed by the tree structure consisting of carry merge logic (CM1 … CM4) to produce the group carries (c_4, c_8, c_{12}) for every 4th bit position. Each carry merge block generates group generate and group propagate signals for a group of two bits:

$$G_{i:j} = G_i + P_i \cdot G_{i-1:j}, \tag{4}$$

$$P_{i:j} = P_i \cdot P_{i-1:j}. \tag{5}$$

Combining the carry merge stages according to Fig. 4 results in the desired 4-bit group carries:

$$c_m = G_{m-1:0} + c_0 \cdot P_{m-1:0} = G_{m-1:0}. \tag{6}$$

4-bit conditional sum adders speculatively generate two sets of sums in the noncritical section in parallel. They assume an input carry of zero and one from the 4-bit groups. Once the group carries are determined by the tree the correct sums are chosen out of the sets via multiplexers. The use of 4-bit

conditional sum adders results in the sparse tree. Most of the carry merge logic can be moved out of the tree to the noncritical section. Thus the maximum fanout stems from two carry merge blocks in the tree structure. The conditional sum adders can be realized using a ripple carry scheme with two rails for the possible input carries. The first conditional sum adder can be simplified with an input carry of $c_0 = 0$.

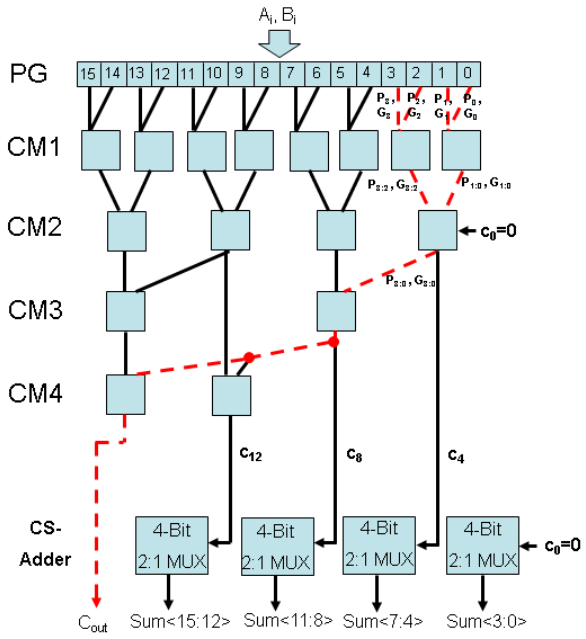

Figure 4. *Structure of the 16 bit sparse-tree adder*

B. *Modifications for Subtraction*

The structure in Fig. 4 has to be adapted to a subtraction. Using 2K-arithmetic a subtraction can be realized by inverting the inputs B_i and setting the incoming carry c_0 to one. The incoming carry has to be taken into account at the first conditional sum adder for sum positions s<3:0> and the carry merge block CM2 for the first 4-bit group:

$$c_4 = G_{3:0} + P_{3:0}. \qquad (7)$$

One can simplify the first conditional sum adder since the input carry is tied to one. Further optimization can be done in the tree structure according to Fig. 5 since no carry out signal is needed. This is due to the internal 16-bit extension.

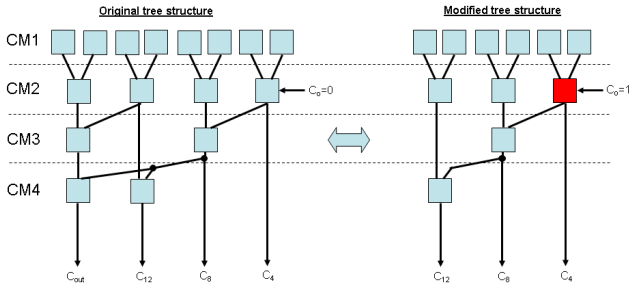

Figure 5. *Modified tree structure for the 16 bit subtraction*

IV. SIMULATION RESULTS

Simulations are based on transistor-level gates in a 65 nm standard CMOS technology at a supply voltage of 1.0 V. Transient simulations of the modulator were done with Ultrasim. The spectrum of the output signal is calculated with a 16384-point FFT and the Hann-window. Fig. 6 shows the power spectrum from zero Hertz to $f_s/2$. The frequency range around the center frequency is drawn with a larger scale in Fig. 7. A bandwidth of 20 MHz is marked with dashed vertical lines.

Fig. 8 shows the SNR for the binary modulator output for a bandwidth range up to 60 MHz, the total bandwidth of the UMTS downlink band at 2.14 GHz. The SNR at 20 MHz bandwidth is 74 dB.

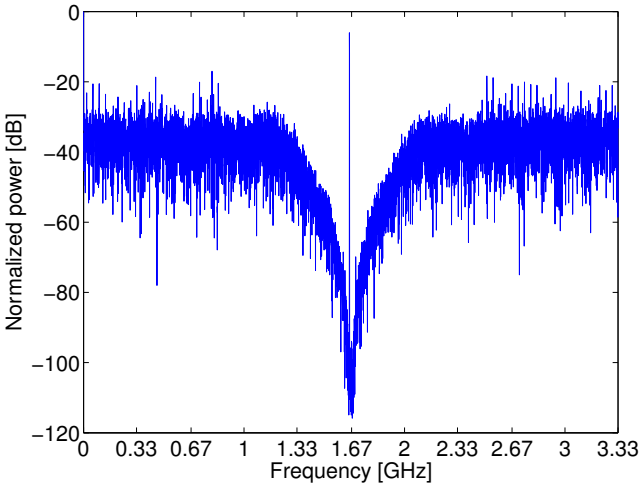

Figure 6. *Modulator output spectrum*

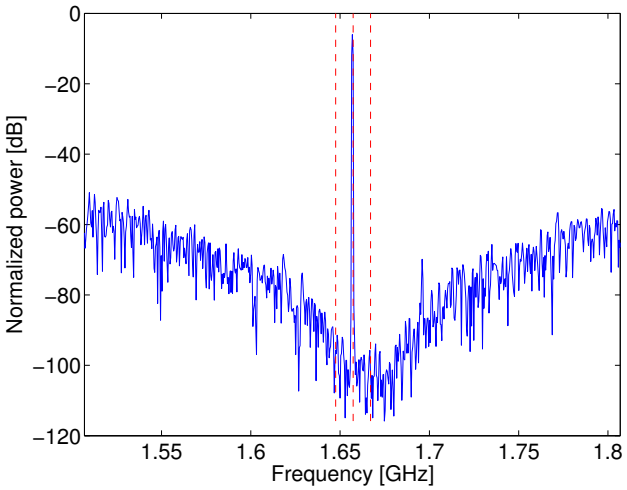

Figure 7. *Modulator output spectrum with bandwidth markers at ±10 MHz offset from the signal.*

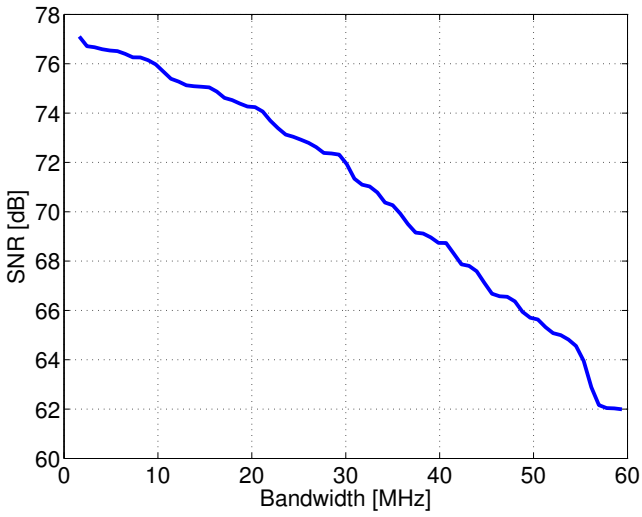

Figure 8. *Signal-to-noise-ratio versus bandwidth*

V. CONCLUSION

In this paper design considerations for a digital bandpass delta-sigma modulator for class-S power amplifiers are given. A time-interleaved architecture of the modulator is proposed and a concept for the high speed implementation of the arithmetic operations is described. This allows for signal frequencies of up to 1.67 GHz at a sampling frequency of 6.67 GHz. The simulated SNR of the binary output is 74 dB for a bandwidth of 20 MHz. This complies with the requirements of 3GPP (3rd generation partnership project). Due to the use of static CMOS logic power consumption using this concept will be around 55 mW. Faster logic families and a faster CMOS technology will provide for the higher sampling frequencies needed for UMTS applications at 2.14 GHz.

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