Continuous-Time Bandpass Delta-Sigma Modulator with 8 GHz Sampling Frequency

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***Abstract*—This paper presents a concept for a Continuous-Time Bandpass-Delta-Sigma Modulator (CT BPDSM) for class-S amplifiers. Class-S amplifiers are very efficient for signals with high dynamic range and are considered to be one possible replacement for conventional linear amplifiers in RF transmitters. A multi-feedback architecture with return-to-zero (RZ) and half-return-to-zero (HRZ) pulses is chosen for the modulator. Noise considerations lead to a low noise transconductor with emitter degeneration. The loop filters consist of LC resonators with Q-enhancement. The effect of excess-loop-delay is mitigated by an optimized clock tree. For a 2.1 GHz input signal an SNR of 59 dB at a bandwidth of 20 MHz is expected.**

I. INTRODUCTION

Many European countries are covered by a close mesh of GSM base stations (Global System for Mobile Communications). With the advent of enhancements to GSM like EDGE (Enhanced Data Rates for GSM Evolution) and the next generation standard UMTS (Universal Mobile Telecommunication System) existing base stations have to be reequipped and new base stations have to be built.

Unlike the constant envelope modulation in GSM modern communication schemes exhibit a much higher dynamic range. This turns out to be a severe problem for power amplifiers (PA) in the transmission chain: The higher the dynamic range the higher the back-off a linear PA has to provide and thus the lower the power efficiency will be. The class-S concept is seen as a possible solution to provide high dynamic range at good power efficiency [1, 2].

A conventional RF transmission chain is depicted in Fig. 1. The baseband signal is converted to analog at the very left of the chain. An IQ-modulator mixes the I and Q part of the signal to the intermediate frequency (IF). Another mixer moves the signal to the carrier frequency. Harmonics are filtered out and the signal is amplified by a linear PA.

The filter and the power amplifier can be replaced by the class-S amplifier in Fig. 2. The concept comprises a CT BPDSM, a switching-mode amplifier and its driver and finally a reconstruction filter. The CT BPDSM generates a fast alternating bitstream from the analog RF signal. The digital output signal of the modulator is amplified by a switching-mode PA. Then desired RF signal is reconstructed from the switching-mode PA output signal with a high-Q bandpass filter.

This work describes the CT BPDSM which plays a key role in the concept. The paper is organized as follows: In Section II the architecture of the modulator is introduced. The circuit design of the most important components is treated in Section III. In Section IV simulation results are presented and Section V concludes the work.

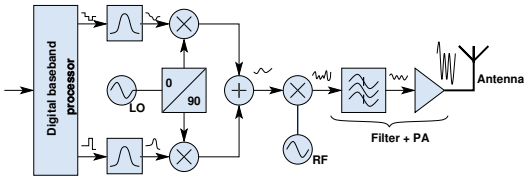

Figure 1. *Block diagram of a conventional transmission chain*

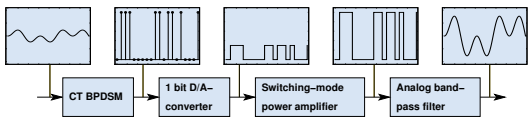

Figure 2. *Block diagram of a class-S amplifier*

II. SYSTEM ARCHITECTURE

The design procedure of a CT BPDSM can be divided into two steps: First, a discrete-time model of the modulator with the desired signal transfer function and noise transfer function is derived. In the second step an impulse-invariant transform is applied to the discrete-time model: The feedback loop is cut at the comparator and the resulting open-loop impulse response is transformed to the continuous-time domain. Now, an equivalent CT BPDSM with identical open-loop impulse-response can be designed [3-5].

While this is straightforward for lowpass delta-sigma modulators, a problem of controllability occurs for bandpass LC delta-sigma modulators. The problem is solved by

introduction of a second feedback pulse into each resonator [5, 6].

Possible feedback pulses for this multi-feedback topology are shown in Fig. 3. If a nonorthogonal pair of pulses is chosen for each resonator the required DAC (Digital-to-Analog-Converter) currents are higher than for orthogonal pairs. A rise of current consumption and noise level is the inevitable result. Therefore a pair of Return-to-Zero (RZ) and Half-Return-to-Zero (HRZ) pulses is chosen for this design.

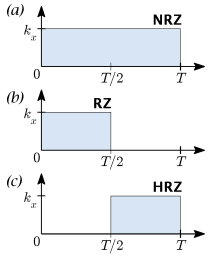

Figure 3. *Feedback pulses: (a) Non-Return-to-Zero, (b) Return-to-Zero and (c) Half-Return-to-Zero*

III. CIRCUIT DESIGN

A block diagram of the modulator on component level is depicted in Fig. 4. Summation of the input signal with the feedback signal is best done by currents. Thus the transconductor G_m converts the input voltage into a current which adds up in the resonator with the feedback currents k_{2r} and k_{2h}. The current sum transforms to a voltage according to the resonator transfer function. A second transconductor G_m feeds an identical resonator with a current proportional to the voltage of the first resonator. Again feedback currents k_{1r} and k_{1r} are added to the transconductor current.

The comparator consists of a preamplifier (preamp) and two latches. It samples and quantizes the voltage of the preceding resonator. The feedback is delayed by either one or two additional latches. The introduced digital delays of a half clock cycle and one clock cycle correspond to the RZ and HRZ feedback pulses, respectively.

A. Nonidealities

A couple of nonidealities are known to occur in BPDSMs. They are named here along with their effect on the modulator performance. Remedies will be given in following section.

- Circuit noise must be kept low. Low noise topologies should be used.
- Kickback effect occurs at components with low input impedance.
- Gain nonlinearity of the transconductors generates harmonics of third order. This reduces the maximum input voltage to the transconductor.
- Excess-loop-delay is the additional, erroneous delay to the feedback signals which is introduced by delays in the comparator and the DAC.
- Metastability of the comparator leads to nondeterministic delay of the feedback and an incorrect output bitstream.
- Low jitter is especially important in oversampling data converters [7].

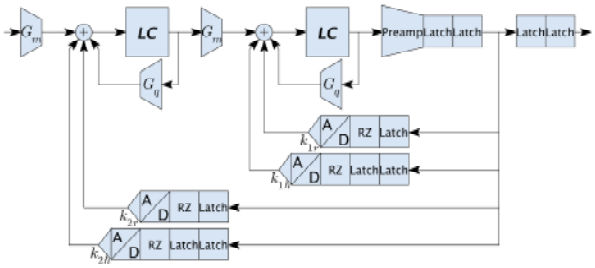

Figure 4. *Component level block diagram of a fourth-order CT BPDSM*

B. Transconductor

Fig. 5 shows two topologies of emitter degenerated transconductors. The transconductor in Fig. 5 (a) requires a higher supply voltage due to the series resistor. The alternative in Fig. 5 (b) exhibits more circuit noise. Here, the two current sources generate noise into both complementary outputs separately. For the transconductor with series degeneration only the series resistors have a significant noise contribution. The noise of the common current source is a common mode effect at the output and thus has no effect on the differential output signal. In this design the difference in noise power was simulated to be 4.6 dB, therefore the transconductor in Fig. 5 (a) is chosen for this design.

In order to reduce undesired feedback between the resonators an emitter follower precedes the actual transconductor (Fig. 6). This increases the input impedance significantly.

The minimum input voltage of G_m depends on the input referred noise of the transconductor. The maximum input voltage is limited by the nonlinearity of the transconductor: The power of induced harmonics must stay well below the minimum input power. For a high SNR the voltage at the resonators has to be maximized. Therefore linearity of the transconductors should be made as high as the associated higher power consumption can be tolerated. The transconductance of the input G_m versus its input voltage is plotted in Fig. 6.

C. Q-enhanced resonator

Integrated *LC* resonators have a poor Q-factor due to resistive losses of the on-chip inductance. These can be compensated by a *Q*-enhancement transconductor G_q of the same topology as G_m.

The capacitance and thus the center frequency of the resonator can be tuned by a differential varactor diode. Fig. 9 shows the normalized resonator voltage versus frequency for an ac-current excitation. The Q-enhancement achieves a Q-factor of 66.

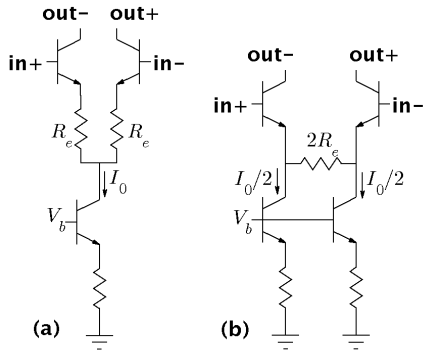

Figure 5. *Two types of emitter degenerated transconductors. (a)series degeneration, (b) shunt degeneration.*

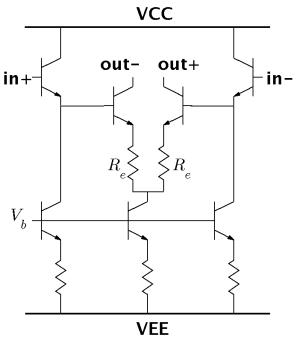

Figure 6. *Transconductor with emitter follower*

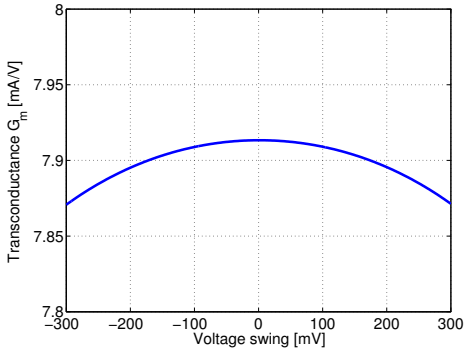

Figure 7. *Transconductance of the input transconductor G_m*

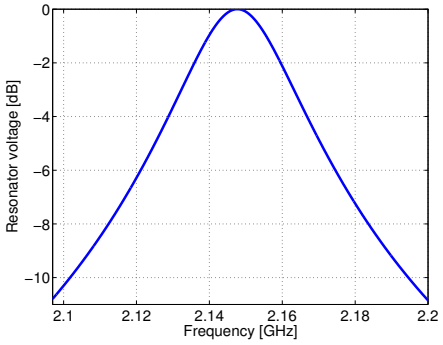

Figure 8. *Normalized resonator voltage of the Q-enhanced resonator*

D. Comparator and feedback

The comparator consists of a preamplifier and two latches. The preamplifier resembles the transconductor with load resistors. High linearity is of no importance to the decider. Therefore the emitter series resistance is removed.

The preamplifier serves two reasons. First, it prevents the kick-back effect and second it helps to reduce metastability of the comparator.

E. Clock tree

The modulator performance is highly sensitive to incorrect timing of the feedback pulses. The clock tree is therefore threefold optimized: Jitter depends on the transition time of the clock signal and the number of amplifiers from the input. Therefore it can be minimized by designing the clock tree amplifiers for high bandwidth and high gain. This reduces the number of necessary amplifiers and the settling time equally.

Second, the clock tree is signal flow oriented, i.e. the clock and the input signal traverse the same length in the same direction.

Finally, the comparator clock is slightly delayed with respect to the sampling clock at the DAC, i.e. the digital delay of the latches is reduced and the feedback signal arrives earlier at the DAC. This compensates for excess-loop-delay, i.e. undesired delay from the comparator preamplifier and the DAC.

IV. Simulation Results

The design was simulated with Spectre. The transient noise simulation includes signal degradation due to noise and on-chip clock jitter. The voltage swing of the input signal is 33 mV, the output voltage swing is 300mV. The circuit dissipates 290 mW from a power supply of 2.5V. The clock frequency of 8 GHz is slightly smaller than for a $f_s/4$ modulator. Four control currents are needed for HRZ and RZ pulses into the two resonators. The varactor voltages of the resonators can be set externally.

Fig. 9 shows the output spectrum of a 16384-point FFT with Hann-window. In Fig. 10 the region around the notch in the transfer function is redrawn. Three vertical dashed lines mark the input signal frequency and the limits of a 20 MHz bandwidth. Finally the dependence of SNR on bandwidth can be seen in Fig. 11. The SNR at a bandwidth of 20 MHz is 59 dB. It decreases to 53 dB at 60 MHz bandwidth.

V. Conclusion

A design of a fourth-order continuous-time bandpass delta-sigma modulator for signal frequencies at 2.1 GHz was presented. Circuit noise of two emitter degenerated transconductors was compared The design features *Q*-enhancement for *LC* resonators and an optimized clock tree to mitigate excess-loop-delay. Metastability is suppressed by a preamplifier preceding the comparator and by additional latches at the output. Simulations indicate an SNR of 59 dB at a bandwidth of 20 MHz.

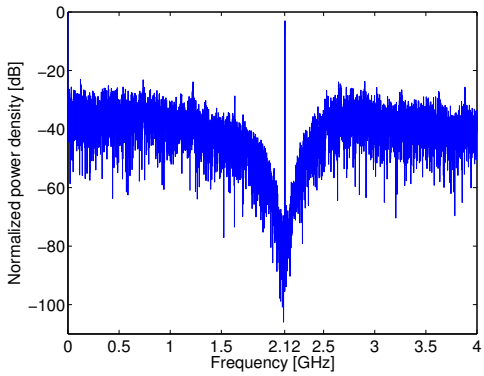

Figure 9. *Modulator output spectrum*

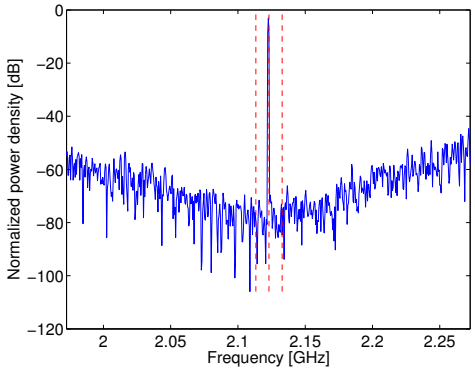

Figure 10. *Larger scale of the output spectrum around the input signal frequency. Dashed lines indicate a ±10 MHz offset from the center frequency.*

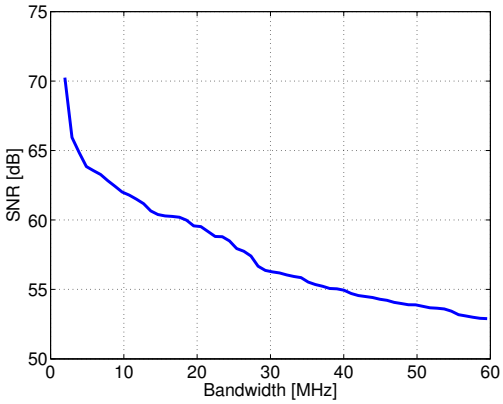

Figure 11. *Signal-to-noise-ratio versus bandwidth*

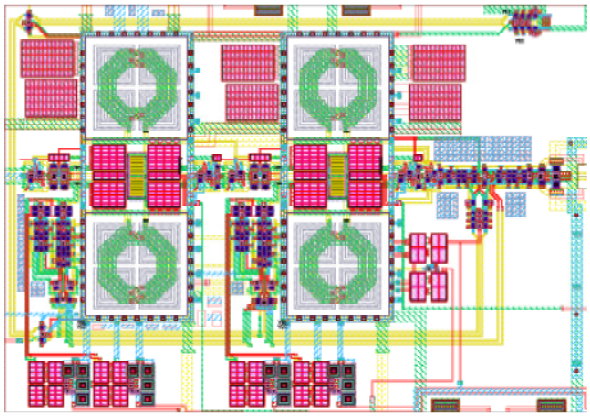

Figure 12. *Modulator core*

ACKNOWLEDGMENT

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