High-Speed ADC Building Blocks in 90 nm CMOS

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***Abstract*— A sample & hold circuit, a comparator and a decision flip-flop are implemented in 90 nm standard CMOS technology. The input switch of the sample & hold circuit provides a bandwidth in excess of 30 GHz at a sampling rate of 10 Gs/s. The limiting amplifier based comparator with active peaking performs slicing of 10 Gbaud signals with a 5%-to-95% settling time of 43 ps. A decision flip-flop provides a phase margin of 324° at 200 mV and 274° at 50 mV input signal swing. All blocks are implemented without any spiral inductors. The building block performance indicates the feasibility of a 40-Gs/s 3-bit flash analog-to-digital converter with 4-fold time-interleaved architecture.**

I. INTRODUCTION

Cost-effective electronic equalization is a major topic in 10 to 40 Gbit/s fiber-optic systems, as fiber dispersion limits the maximum transmission distance. The increased flexibility and the possibility of maximum-likelihood sequence estimation are arguments for the use of digital equalizers instead of the more mature analog transversal equalizers. The main circuit design challenge of the digital equalizer is the high-speed analog-to-digital converter (ADC). Fortunately, only a relatively low resolution in the range of 3 to 4 bits is required [1,2].

The fastest ADC reported to date is a 3-bit 40-Gs/s ADC-DAC combination in SiGe technology that offers 12 GHz input bandwidth [3]. The fastest ADC implemented in CMOS achieves 8 bit resolution at 20 Gs/s with an input bandwidth of 6 GHz [4]. It uses 80 time-interleaved converters and a preamplifier implemented in BiCMOS technology.

In this work, basic ADC building blocks are implemented to evaluate the feasibility of a CMOS ADC with a conversion rate of 40 Gs/s and 3 bit resolution. A moderate parallelized 4-fold time-interleaved architecture is considered, resulting in a sampling rate of 10 Gs/s for the individual flash ADCs. The second section of this paper introduces the target time-interleaved ADC concept. The third section describes the design of the individual circuit blocks and section 4 presents the experimental results. A conclusion is given in section 5.

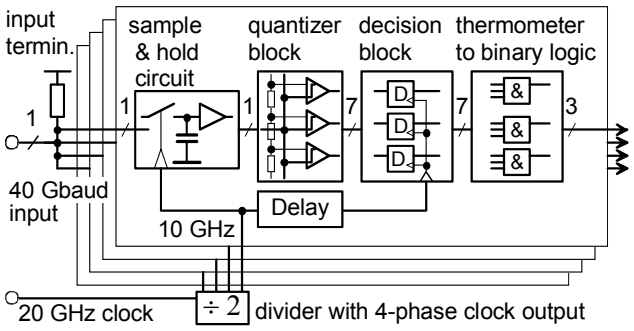

Figure 1. Concept of a 40-Gs/s ADC consisting of four time-interleaved 10-Gs/s flash ADCs.

II. ADC CONCEPT

Figure 1 shows the basic concept of the target 4-fold time-interleaved flash ADC. Four time-interleaved samplers perform analog demultiplexing of the 40 Gbaud input data stream into four analog 10 Gbaud continuous-value discrete-time data streams. The input bandwidth of the samplers is most critical, as the hold capacitor voltage has to follow the 40 Gbaud input signal during track phase. The output bandwidth requirement of the following buffer is relaxed, as it already operates on the demultiplexed 10 Gbaud data stream. The buffer drives the quantizer block consisting of 7 comparators. This quantizer block does a continuous-time comparison of the buffered input voltage with the 7 quantization thresholds that are generated by a resistive divider ladder. A flip-flop block performs strobed decisions on the comparator output voltages. The thermometer code flip-flop output signals are further processed by a logic network to provide a binary 3 bit digital signal.

III. BUILDING BLOCK DESIGN

Fully balanced differential signaling is used throughout all blocks. Although the wire and transistor count are doubled, balanced differential signaling relaxes the common mode rejection requirements of the circuits. All building blocks are designed for evaluation within a 50 Ω measurement environment, i.e. the single-ended impedance level of the differential amplifiers is about 50 Ω and

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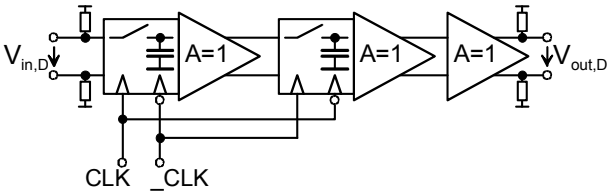

Figure 2. Block diagram of the sample & hold circuit.

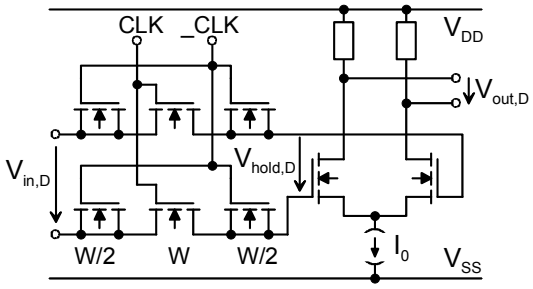

Figure 3. Schematic of the track & hold circuit.

transistors with relatively large gate width are used. Accordingly, the power consumption of the evaluation circuits is relatively large: 40 mV for the sample & hold, 110 mW for the comparator and 100 mW for the flip-flop. The supply voltage is 1.2 V. The saturated single-ended signal swing of the amplifier outputs is 600 mV at the internal nodes and 350 mV at the 50 Ω terminated outputs.

The admittance level of the presented sample & hold circuit has to be divided by four in a complete 4-fold interleaved flash ADC design to maintain the achieved bandwidth at the 50 Ω terminated input node. The admittance levels of the 7-fold parallel comparators and decision flip-flops in the individual flash ADCs have to be scaled down even more in a final ADC design. For circuits that use spiral inductor peaking, the admittance downscaling is difficult, as inductor impedance upscaling requires larger inductors with more windings. This results in increased chip area per block – opposed to the situation without inductors - and reduced inductor self-resonance frequency. The presented circuits are thus implemented without any spiral inductors and allow for straightforward admittance downscaling by reducing the transistor and resistor widths and by using resistors with a larger resistivity per unit square.

A. Sample & hold circuit

The sample & hold circuit shown in Figure 2 consists of two cascaded track & hold circuits in a master-slave configuration and an output buffer. The track & hold sampling switch is a differential n-channel transfer gate that is compensated by dummy gates at both sides as shown in Figure 3. The dummy transistors prevent charge kickback to the input and to the hold voltage when the switch passes from track to hold mode. The hold capacitance is composed of the buffer input capacitance and the hold-side transfer gate capacitance. The transfer gate of the first track & hold has wider transistors than the second one, as the first switch has

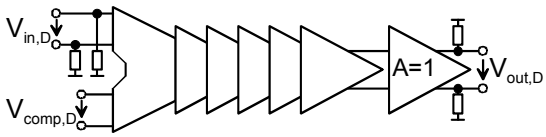

Figure 4. Block diagram of the comparator circuit.

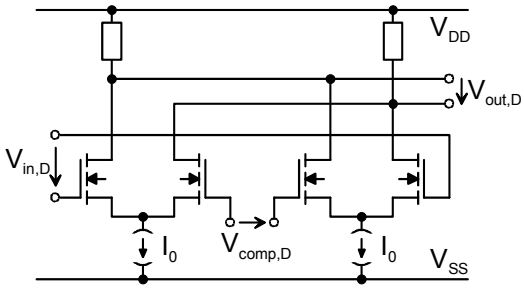

Figure 5. Schematic of the comparator input stage.

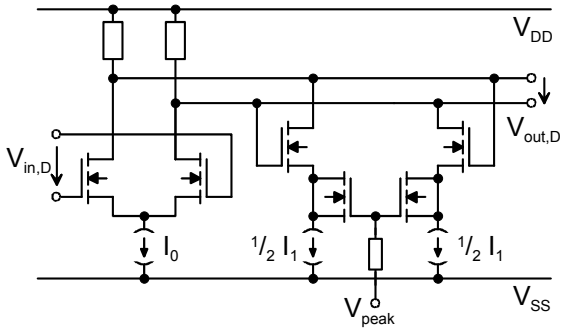

Figure 6. Schematic of the comparator gain stage with active peaking.

to track the 40 Gbaud input signal, whereas the second switch only tracks the already downsampled 10 Gbaud signal. The hold voltage is buffered by differential amplifiers with about unity gain and maximized linear input voltage range. The backside terminated output buffer also provides about unity gain. A single-ended signal swing of ±200 mV around the input common mode level $V_{in,CM}$ is supported, resulting in the capability to handle differential input signals in the range of ±400 mV. The required single-ended clock swing is 1 V with the clock high level set to $V_{clk,H} = V_{in,CM} + 700$ mV for maximized input bandwidth. In a final ADC design, the differential clock signals can be provided by pairs of full-swing CMOS inverters that are connected to bootstrap circuits. In the implemented evaluation circuit, the clock is applied externally to provide flexibility for testing.

B. Comparator circuit

The comparator block shown in Figure 4 consists of an input compare stage, a five stage limiting amplifier and an output buffer. In contrast to other comparator designs [5], the strobed decision function is not included in the comparator stage, it is shifted to following decision flip-flops. The input stage compares the high-speed input signal $V_{in,D}$ with the voltage V_{compD}. It consists of two differential amplifiers that sum up their output currents at common load resistors as shown in Figure 5. The limiting function is

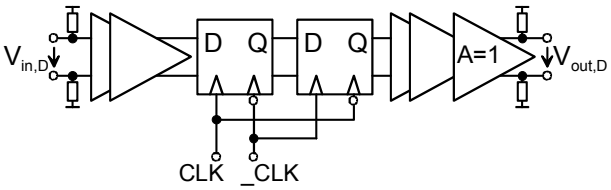

Figure 7. Block diagram of the flip-flop circuit.

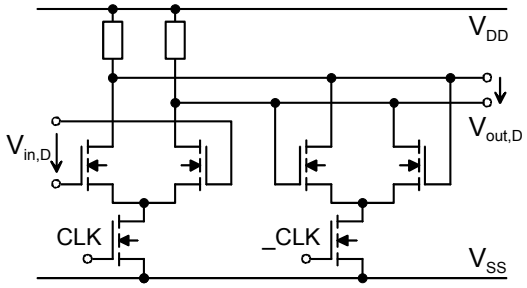

Figure 8. Schematic of the D-latch.

implemented with a chain of high-speed low-gain differential amplifiers, as shown in Figure 6. As the output voltage settling time of a conventional limiter chain is significantely decreased for a small difference between the voltages $V_{in,D}$ and V_{compD}, adjustable active peaking is added to each limiter stage to provide extra dynamic gain. The peaking circuitry consists of a cross-coupled capacitively source degenerated differential pair. The degeneration capacitance is implemented with MOSFETs and can be adjusted by the voltage V_{peak}.

C. Decision Flip-Flop

The flip-flop circuit shown in Figure 7 consists of two preamplifier stages, a master-slave connection of two D-latches, two postamplifier stages and an output buffer. The CML-latches are shown in Figure 8. The latches are optimized for high-speed operation by omitting the common current source that would require same valuable part of the narrow voltage headroom. The master and the slave latch are dimensioned individually for optimum speed and switching performance. The required single-ended clock signal swing is 600 mV with the common mode level set to $(V_{DD}-V_{SS})/2$.

IV. Experimental Results

The building blocks are tested on-wafer. The differential 10 GHz clock and data input signals are provided by a Anritsu MP1763C pulse-pattern generator. A differential 40 Gbit/s data stream is provided by a SHF 404 4-to-1 MUX with decorrelated 10 Gbit/s PRBS data streams applied to the MUX inputs. Figure 9 shows the sampling of a 40 Gbit/s input data stream with a 10 GHz clock by the sample & hold circuit. The logic high- and low-levels are widened, as the sample & hold circuit intentionally must not regenerate the distorted input signal. The trails visible in the eye diagram of the PRBS 2^7-1 output signal show that the widening is not due to random noise, but due to data pattern dependant signal distortion. The distortion is caused by the limited bandwidth

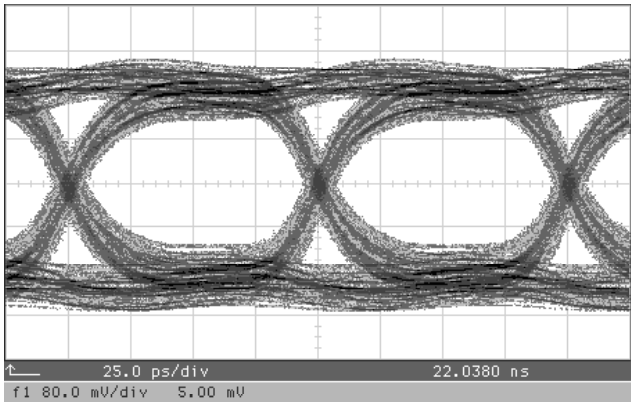

Figure 9. Measured sample & hold circuit output eye diagram with a 40 Gbit/s PRBS 2^7-1 input data stream at f_{clock} = 10 GHz.

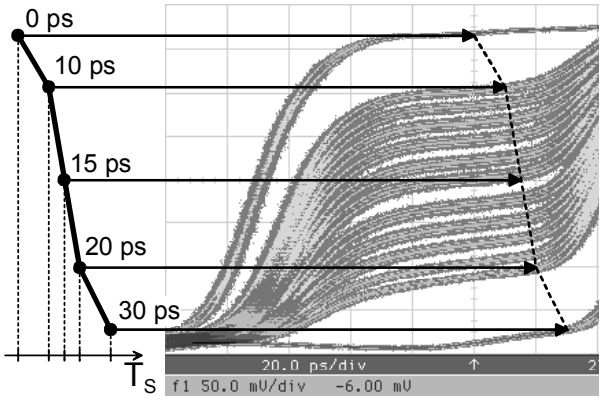

Figure 10. Reconstruction of the hold voltage $V_{hold,D}(t)$ of the first track & hold stage in track mode by varying the sampling time T_S.

of the 40 Gbit/s signal source, by the first and second track & hold circuits, and by the signal interconnect paths. To evaluate the bandwidth of the first track & hold transfer gate, the sampling time is varied in steps of 1 ps on a specific edge of the 40 Gbit/s input signal to reconstruct the input hold signal $V_{hold,D}(t)$, as illustrated in Figure 10. The detected 20%-to-80% hold voltage rise time is between 11 and 12 ps at $V_{clk,H} = V_{in,CM} + 0{,}7$ V, whereas the applied MUX signal provides edges with 9 ps 20%-to-80% rise time. The approximated rising edge waveform $V_{in,D}(t)$ of the 50 Ω terminated 40 Gbit/s input signal is applied to an RC-lowpass in a SPICE simulation. The RC-bandwidth is adjusted for 12 ps risetime of the lowpass output signal. In the simulation, the 12 ps rise time corresponds to a -3 dB bandwidth of 32 GHz. The random aperture jitter is estimated to 130 fs by measuring the hold voltage amplitude noise when sampling the steepest part of the input edge. The large-signal gain of the cascaded buffer chain with a ±400 mV differential input signal is 0.9 times the small-signal value. The track-to-hold parametric gain ratio is 0.965 and the track & hold circuit signal feedthrough ratio is 0.018.

The DC quantization characteristic of the comparator is shown in Figure 11. The slicing characteristics are uniformly for compare voltages $V_{comp,D}$ ranging from -300 mV to

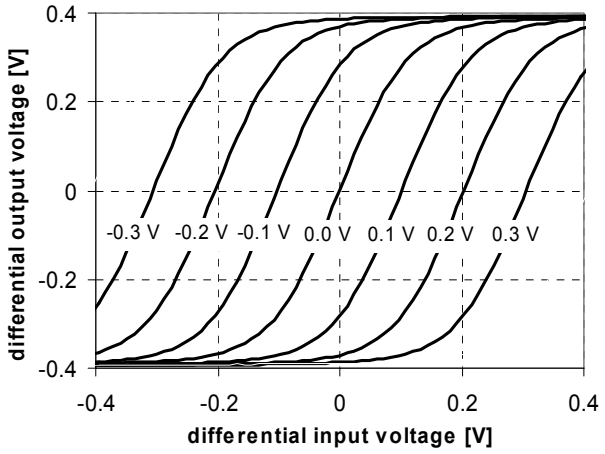

Figure 11. Measured comparator DC quantization characteristic with differential compare voltage $V_{comp,D}$ = -0.3 V to 0.3 V as parameter.

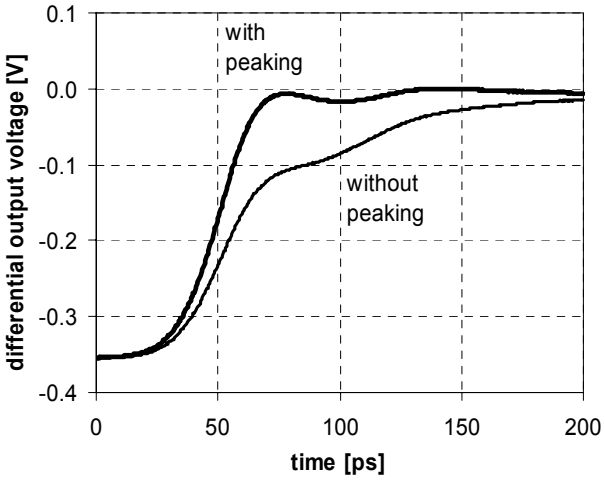

Figure 12. Measured comparator output voltage transient $V_{out,D}(t)$ with peaking enabled ($V_{peak} = V_{DD}$) and disabled ($V_{peak} = V_{SS}$). $V_{in,D}$ step from -500 mV to 0 mV at $V_{comp,D}$ = 0 mV.

+300 mV. Thus, slicing of a ±400 mV range differential input signal with 3 bit quantization can be expected at least. Figure 12 shows the effect of the active peaking on the settling time behavior of the output voltage. The input voltage $V_{in,D}$ does a transition from a value that has a 500 mV offset from the compare voltage $V_{comp,D}$ to zero offset from $V_{comp,D}$. This is the worst case for the comparator output voltage settling time. The 5%-to-95% settling time is improved from 111 ps without peaking to 43 ps with the peaking enabled.

Figure 13 shows the measured phase margin of the decision flip-flop versus single-ended input signal swing. The phase margin is measured with a PRBS 2^{31}-1 input data stream for a BER < 10^{-12}. The phase margin is 274° at 10 GHz decision rate with a flip-flop input signal swing of 50 mV, which corresponds to a ±1/7 LSB swing around the slicing threshold at the comparator circuit *input* with ±400 mV differential input range and 3 bit resolution.

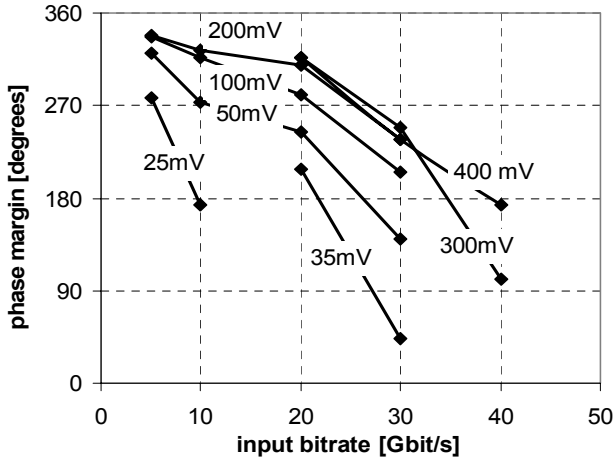

Figure 13. Phase margin of flip-flop versus input bit rate. Single-ended input voltage swing as parameter. $f_{Toggle} = f_{bit}$ @ 5, 10 Gbit/s. $f_{Toggle} = ¼ f_{bit}$ @ 20, 30, 40 Gbit/s.

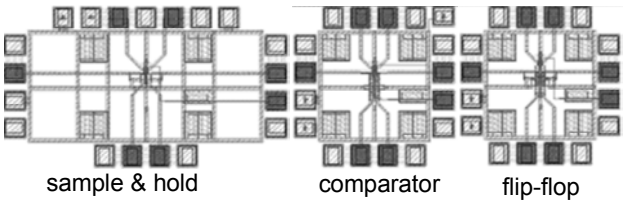

Figure 14. Layout of the ADC building blocks. Pad pitch 100 µm.

V. Conclusion

Basic ADC building blocks implemented in 90 nm CMOS technology are evaluated. The sample & hold circuit samples 40 Gbit/s input signals with a rate of 10 GHz and an input sampler bandwidth of 32 GHz. The comparator and the decision flip-flop offer enough speed, sensitivity and settling time performance for 10 Gs/s operation in the interleaved individual flash converters. Due to the lack of any spiral inductor peaking, the building blocks are suited for admittance downscaling in a complete ADC design. Remaining design challenges for the complete ADC design are the 4-phase 10 GHz clock generation and distribution, the precise relative timing of the sample & hold circuit and the decision flip-flops, and the symmetrical front-end integration of four time-interleaved sample & hold circuits.

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